SA400
minifloppy™
Diskette Storage Drive

OEM Manual

Shugart Associates

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PREFACE

This manual describes the electrical and mechanical characteristics of the SA400 minifloppy™drive required by customers who purchase it as an OEM device. It contains the timing, electrical and mechanical specifications; recommended formats and circuitry necessary to interface it to a host controller/formatter.

For maintenance information, reference the SA400 Service Manual, P/N 54096.

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FIGURE 1. SA400 MINIFLOPPY DRIVE

1.0   INTRODUCTION

The SA400 minifloppy™drive offers the system designer the random access storage capability of floppy disk drives in a package the size of most cassette tape units. It also provides superior data integrity and faster throughput of data when compared with cassette drives.

The SA400 is based on the proven floppy disk drive technology of the Shugart SA800 drive. It features a unique new direct drive stepping motor actuator, utilizing a spiral cam with a v-groove positive detent which assures precise location of the read/write head on a track. The drive employs the same proprietary glass bonded ferrite/ceramic read/write head as the SA800 uses. AC power requirements have been eliminated through the use of a DC servo-controlled spindle drive motor. The drive is also equipped with an interface which allows upward expansion of the units within the system and future system enhancements with the large floppy drive.

Applications for the minifloppy drive include word processing and text editing systems; mini and micro computer program storage; power typing systems; "intelligent" desktop calculators and the microcomputer hobby market.

The SA104/105 minidiskette™media used with the SA400 is similar to the standard flexible disk, only smaller. It is available for soft (SA104) or hard (SA105) sectored formats. The minidiskette diameter is 5.125 inches (130.2 mm) and the jacket is a square 5.25 inches (133.4 mm).

1.1 Specification Summary

1.1.1 Performance Specifications

Capacity
Unformatted
per disk	109.4K bytes
per track	3125 bytes

Formatted (Reference Section 7.0)

	Soft Sectoring	Hard Sectoring
per disk	80.6K bytes	72.03K bytes
per track	2304 bytes	2058 bytes
per sector	128 bytes	128 bytes
sectors per track	18	16

Transfer Rate	125.0K bits/sec.
Latency (average)	100 ms

Access Time
track to track	40 ms
average	463 ms
settling time	10 ms
Head Load Time	75 ms
Disc Motor Start Time	1 sec.

1.1.2 Functional Specifications

Rotational Speed	300 RPM
Recording Density (inside track)	2581 BPI
Flux Density	5162 FCI
Track Density	48 TPI
Tracks	35
Inside Track Radius	1.542 in. (3.916 cm)
Outside Track Radius	2.250 in. (5.715 cm)
Index	1
Encoding Method	FM
Media Requirements	SA 105 or SA107 minidiskette (Hard Sectored) SA104 minidiskette (Soft Sectored)

1.1.3 Physical Specifications

Environmental Limits:
Ambient Temperature =

Operating	Shipping	Storage
40°F to 115°F	-40°F to 144°F	-8°F to 117°F
(4°C to 46°C)	(-40°C to 62°C)	(-22°C to 47°C)

Relative Humidity =

20% to 80%	1% to 95%	1% to 95%

Max. Wet. Bulb =
78°F (25°C)	No Condensation

DC Voltage Requirements:
+12 VDC ± 5%	0.9 amp (typical)	1.8 amp (maximum)
+5 VDC ± 5%	0.5 amp (typical)	0.7 amp (maximum)

Mechanical Dimensions:
Width	5.75 in. (14.60 cm.)
Height	3.25 in. (8.25 cm.)
Depth	8.00 in. (20.32 cm.)
Weight	3 lbs. (1.36 kg.)

Power Dissipation =
15 watts (51 BTU/Hr) Operating (typical)
7.5 watts (26 BTU/Hr) Standby (typical)

1.1.4 Reliability Specifications

*MTBF (Mean Time Between Failures)	8,000 Power on Hours (Typical Usage)
PM (Preventive Maintenance)	Not Required
MTTR (Mean Time to Repair)	30 Minutes

Error Rates
Soft Errors	1 per 10^8 bits read
Hard Errors	1 per 10^{11} bits read
Seek Errors	1 per 10^6 seeks
Component Design Life	5 years
Media Life	3.0×10^6 passes per track

*MTBF assumes duty cycle of spindle drive motor to be 25% of POH.

2.0 FUNCTIONAL CHARACTERISTICS

2.1 General Operation

The SA400 minidiskette Storage Drive consists of read/write, control and drive motor electronics, drive mechanism, read/write head, track positioning mechanism, and removable minidiskette. These components perform the following functions:

1. Interpret and generate control signals.

2. Move the read/write head to the desired track.

3. Read and write data.

4. Control drive motor speed.

The interface signals and their relationship to the internal functions are shown in figure 2.

The head positioning actuator positions the read/write head to the desired track on the minidiskette. The head load actuator loads the mini-diskette against the read/write head and data may then be recorded or read.
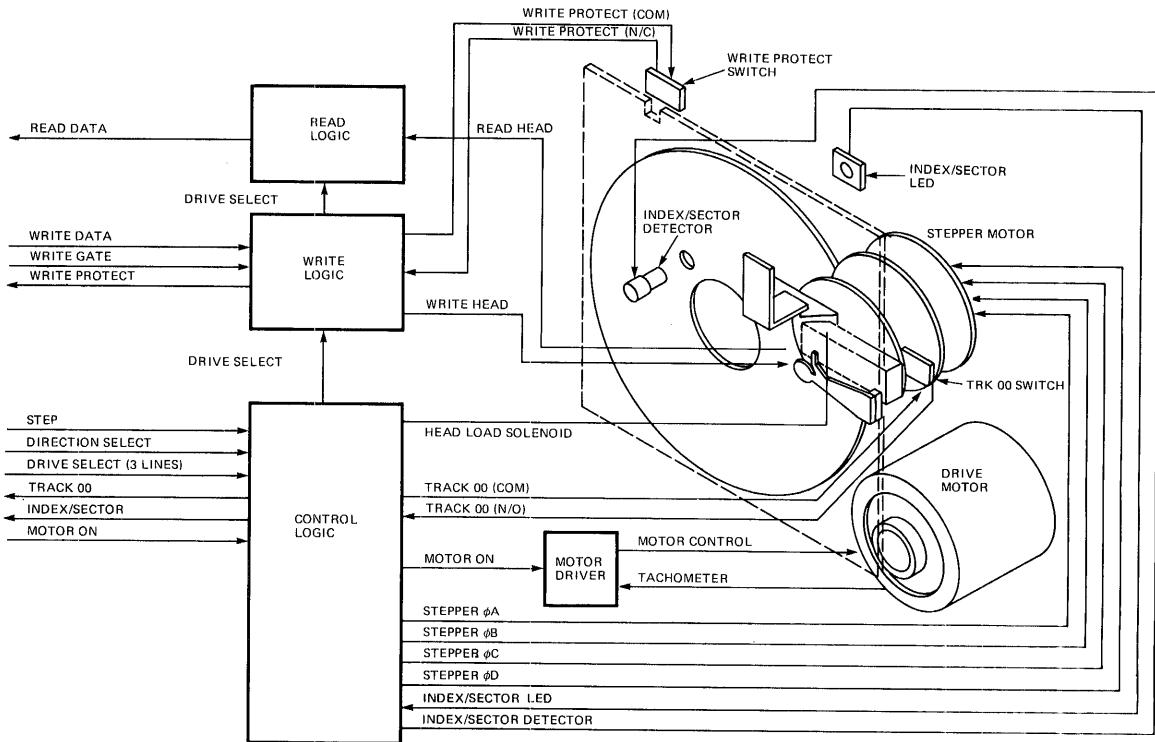
FIGURE 2. SA400 FUNCTIONAL DIAGRAM

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2.2 Read/Write and Control Electronics

The electronics are packaged on two PCB's. The PCB's contain:

1. Index/Sector detector.

2. R/W head position actuator drivers.

3. R/W head load actuator driver.

4. Write current drivers.

5. Read amplifier and transition detectors.

6. Write protect detector.

7. Drive select circuits.

8. Drive motor control circuits.

2.3 Drive Mechanism

The minifloppy drive motor operates on 12 VDC and rotates the spindle at 300 rpm through a belt-drive system. The speed of the motor is controlled by a feed back from a tachometer internal to the motor. A registration hub, centered on the face of the spindle, positions the minidiskette. A hub clamp that moves in conjunction with the door closure mechanism centers and clamps the mini-diskette onto the spindle hub.

2.4 R/W Head Positioning Mechanism

An electrical stepping motor and a face cam positions the read/write head. The stepping motor rotates the cam clockwise or counterclockwise with two step increments per track. The using system increments the stepper motor to the desired track by selecting the proper direction and issuing one step pulse per track. The drive control electronics issues the second step pulse needed per track.

2.5 Read/Write Head

The SA400 R/W head is a single element glass bonded ferrite/ceramic head with straddle erase elements to provide erased areas between data tracks. Thus normal interchange tolerances between media and drives will not degrade the signal to noise ratio and insures minidiskette interchangeability.

The R/W head is mounted on a carriage assembly which moves on rails and is positioned by the cam. The minidiskette is held in a plane perpen-dicular to the R/W head by a platen located on the base casting. This precise registration assures perfect compliance with the R/W head. The mini-diskette is loaded against the head with a load pad actuated by the head load solenoid.

The R/W head is in direct contact with the mini-diskette. The head surface has been designed to obtain maximum signal transfer to and from the magnetic surface of the minidiskette with mini-mum head/minidiskette wear.

2.6 Recording Format

The format of the data recorded on the disk is totally a function of the host system, and can be designed around the users application to take maximum advantage of the total available bits that can be written on any one track.

For a detailed discussion of various recording formats, reference section 7.0.

3.0 FUNCTIONAL OPERATIONS

This section of the manual defines the functional as well as the timing relationships of the operations for the SA400.

3.1 Power Sequencing

Applying DC power to the SA400 can be done in any sequence; however, during power up, the Write Gate line must be held inactive or at a high level. This will prevent possible "glitching" of the media. After application of DC power, a 100 ms delay should be introduced before any operation is performed. Also, after powering on, initial position of the R/W head with respect to the data tracks on the media is indeterminant. In order to assure proper positioning of the R/W head after powering on, a Step Out operation should be performed until the Track 00 line becomes active (Recalibrate).

3.2 Drive Selection

Drive Selection occurs when the Drive Select line is activated. Under normal operation, the Drive Select line will load the R/W head against the mini-diskette enabling contact of the R/W head with the media and will also light a LED on the front plate.

3.3 Motor On

In order for the host system to read or write data the DC drive motor must be turned on. This is accomplished by activating the line -Motor On. A one (1) second delay must be introduced after activating this line to allow the motor to come up to speed before reading or writing can be accomplished.

The motor must be turned off by the host system by deactivating the Motor On line. This should be done if the drive has not received a new command within two (2) seconds (10 revolutions of diskette) after completing the execution of a command. This will insure maximum motor and media life.

3.4 Track Accessing

Seeking the R/W head from one track to another is accomplished by:

1. Activating the Drive Select line.

2. Selecting the desired direction utilizing the Direction Select line.

3. Write Gate being inactive.

4. Pulsing the Step line.

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WRITE GATE

DRIVE SELECT

DIRECTION SELECT

REVERSE

FORWARD

1 μs MIN

1 μs MIN

1 μs MIN

1 μs MIN

STEP

1 μs MIN

1 μs MIN

40 MS MIN

FIGURE 3. TRACK ACCESS TIMING

DC POWER

MOTOR ON

100 MS MIN

DRIVE SELECT

STEP

WRITE GATE

VALID READ DATA

50 MS MIN

100 μs MIN

75 MS MIN

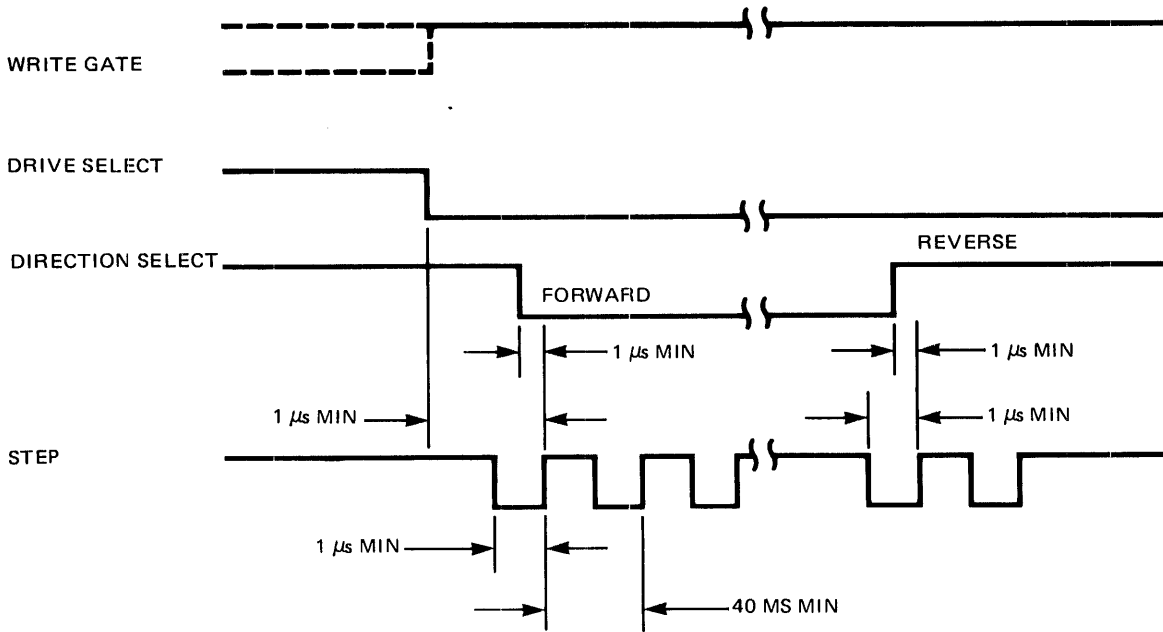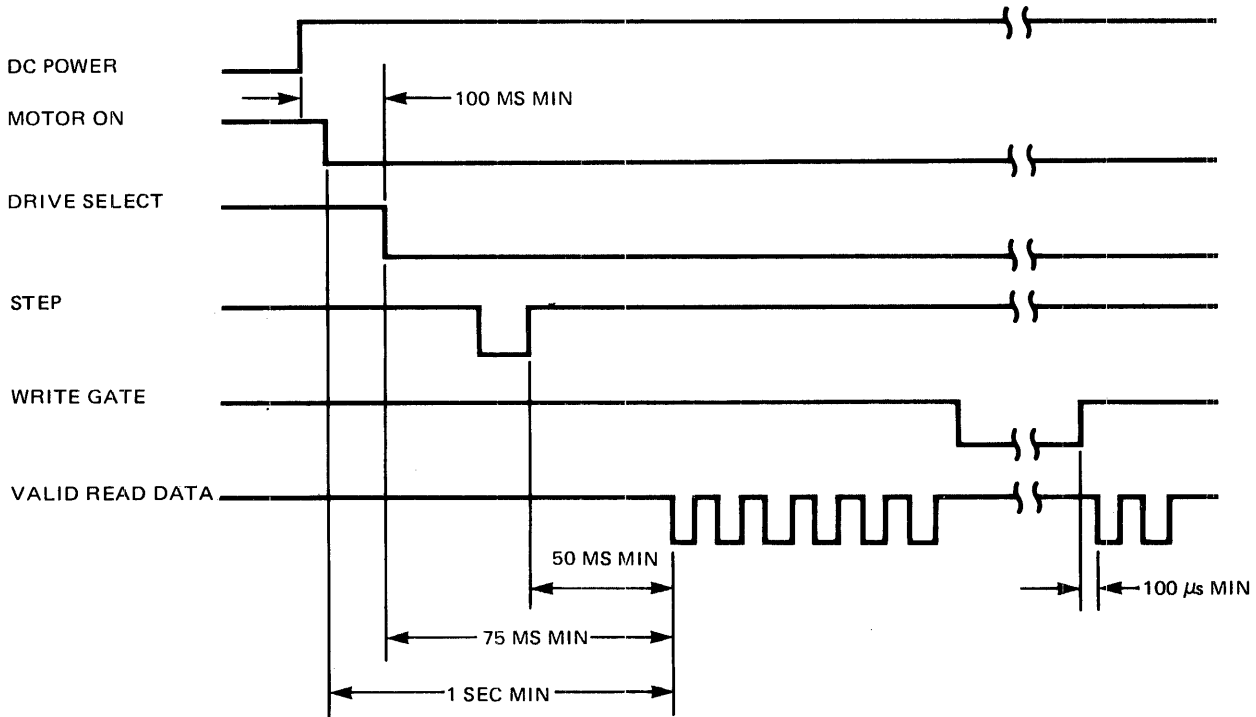1 SEC MIN

FIGURE 4. READ INITIATE TIMING

Multiple track accessing is accomplished by repeatedly pulsing the Step line until the desired track has been reached. Each pulse on the Step line will cause the R/W head to move one track either in or out depending on the Direction Select line. Head movement and direction latching is initiated on the trailing edge of the Step pulse.

During a Recalibrate (Step to Track 00), the worst case number of step pulses required is 58. The worst case occurs when the carriage is positioned IN beyond track 34 and the carriage comes out of the spiral cam groove. In this case, it can take up to 24 steps for the carriage to pick up the groove in the cam and then another 34 steps to reach track 00.

3.4.1 Step Out

With the Direction Select line at a plus logic level (2.5V to 5.25V) a pulse on the Step line will cause the R/W head to move one track away from the center of the disk. The pulse(s) applied to the Step line and the Direction Select line must have the timing characteristics shown in Figure 3.

3.4.2 Step In

With the Direction Select line at a minus logic level (0V to .4V), a pulse on the Step line will cause the R/W head to move one track closer to the center of the disk. The pulse(s) applied to the Step line must have the timing characteristics shown in figure 3.

3.5 Read Operation

Reading data from the SA400 minifloppy drive is accomplished by:

a. Activating Drive Select line.

b. Write Gate being inactive.

The timing relationships required to initiate a read sequence are shown in figure 4. These timing specifications are required in order to guarantee that the R/W head position has stabilized prior to reading.

The timing of Read Data is shown in figure 5.

3.6 Write Operation

Writing data to the SA400 is accomplished by:

a. Activating the Drive Select line.

b. Activating the Write Gate line.

c. Pulsing the Write Data line with the data to be written.

The timing relationships required to initiate a write data sequence are shown in Figure 6. These timing specifications are required in order to guarantee that the R/W head position has stabilized prior to writing.

The timing specifications for the Write Data pulses are shown in figure 7.

3.7 Sequence of Events

The timing diagram shown in figure 8 shows the necessary sequence of events with associated timing restrictions for proper operation.

3.8 Multiplex Option

As shipped from the factory, the drive is set to operate as a single unit or in a non-multiplexed mode. For multiplexed or "daisy chained" operation, the trace labeled "MUX" must be cut.

3.8.1 Drive Selection

In a multiple drive system (trace "MUX" cut), only the drive with its Drive Select line active will load its R/W head, respond to the input lines and gate the output lines.

Three separate input lines, Drive Select 1, Drive Select 2 and Drive Select 3, are provided so that up to three drives may be multiplexed on a single I/O cable in a system. A "Program Shunt" in IC location 1F, position 1, 2 and 3 with designators DS1, DS2 and DS3, has been provided to select which Drive Select line will activate the interface signals for a unique drive. As shipped from the factory this program shunt has the three locations shorted. To set an address on a drive, its location should remain shorted and the other two locations should be cut. For methods of cutting the program shunt traces, reference section 4.1.1.2.

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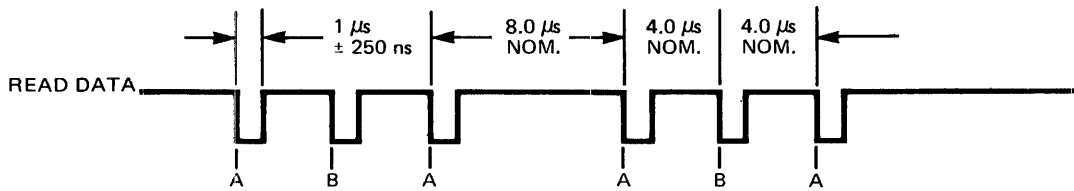
A = LEADING EDGE OF BIT MAY BE ± 800 ns FROM ITS NOMINAL POSITION.
B = LEADING EDGE OF BIT MAY BE ± 400 ns FROM ITS NOMINAL POSITION.

FIGURE 5. READ SIGNAL TIMING
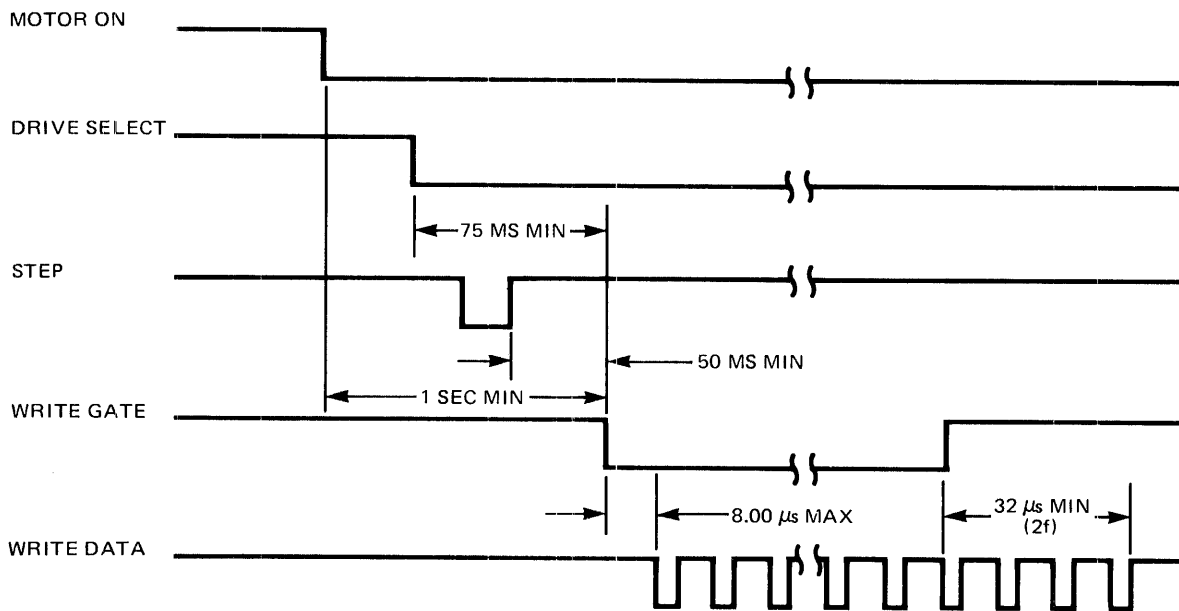
FIGURE 6. WRITE INITIATE TIMING
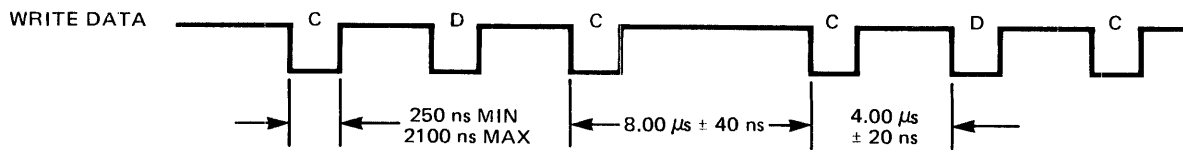
FIGURE 7. WRITE DATA TIMING

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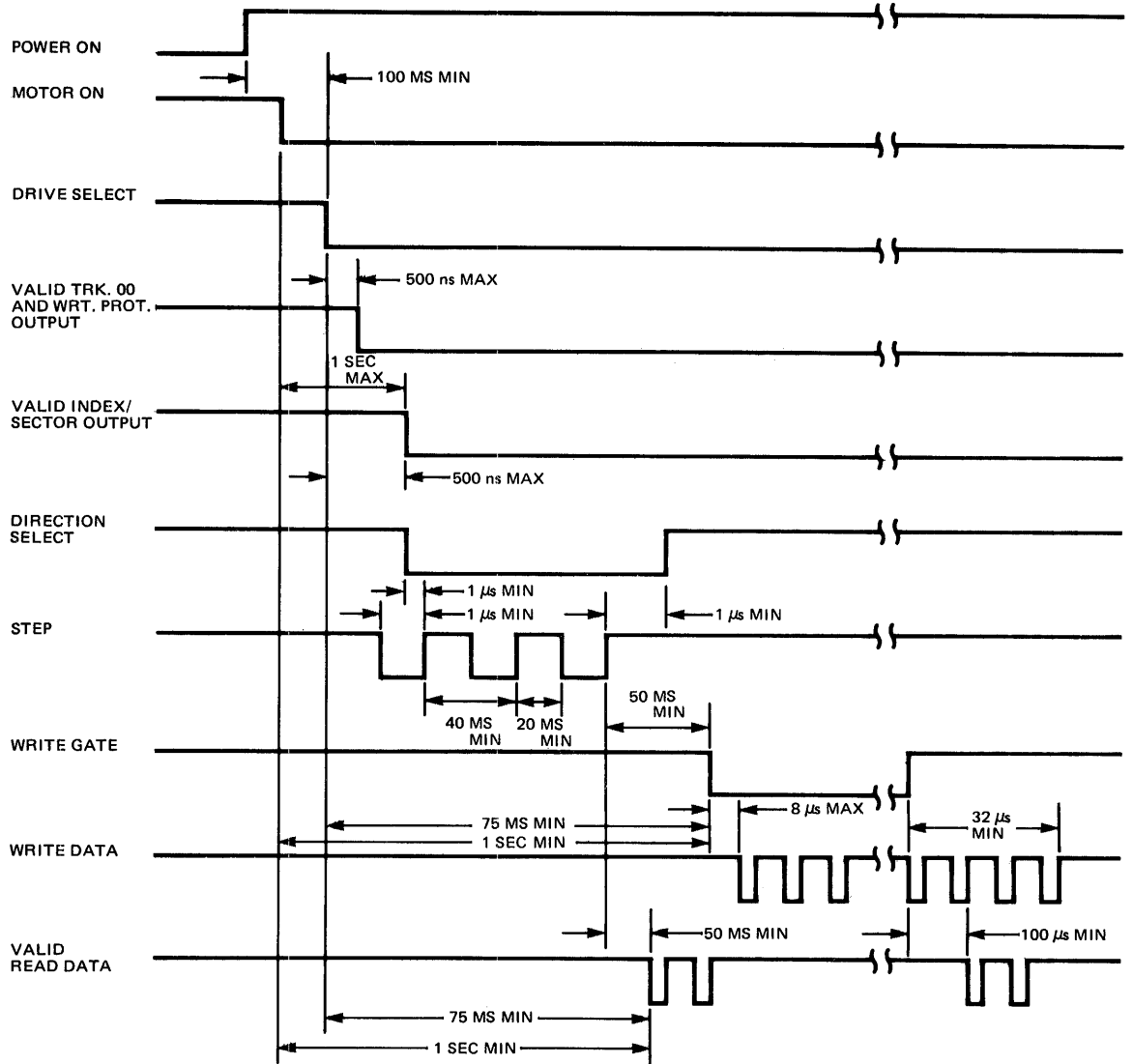
FIGURE 8. GENERAL CONTROL AND DATA TIMING REQUIREMENTS

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4.0 ELECTRICAL INTERFACE

The interface of the SA400 minidiskette drive can be divided into two categories:

1. Signal

2. Power

The following sections provide the electrical definition for each line.

Reference figure 9 for all interface connections.

4.1 Signal Interface

The signal interface consists of two categories:

1. Control

2. Data transfer

All lines in the signal interface are digital in nature and eitner provide signals to the drive (input), or provide signals to the host (output), via interface connector P1/J1.

4.1.1 Input Lines

The input signals are of 3 types, those intended to be multiplexed in a multiple drive system, those which will perform the multiplexing and Motor Control.

The input signals to be multiplexed are:

1. Direction Select

2. Step

3. Write Data

4. Write Gate

The input signals which are intended to do the multiplexing are:

1. Drive Select 1

2. Drive Select 2

3. Drive Select 3

The input lines have the following electrical specifications. Reference Figure 10 for the recommended circuit.

True = Logical zero = Vin ±0.0V to +0.4V
@ Iin = 40 ma (max)

False = Logical one = Vin +2.5V to +5.25V
@ Iin = 0 ma (open)

Input Impedance = 150 ohms

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FLAT RIBBON OR
TWISTED PAIR
MAX 10 FEET

HOST SYSTEM   SA400

J1
7
INDEX/SECTOR
8   9
DRIVE SELECT 1
10   11
DRIVE SELECT 2
12   13
DRIVE SELECT 3
14   15
MOTOR ON
16   17
DIRECTION SELECT
18   19
STEP
20   21
WRITE DATA
22   23
WRITE GATE
24   25
TRACK 00
26   27
WRITE PROTECT
28   29
READ DATA
30

+5 VDC   J2
4   3
+5 RETURN
+12 VDC
1   2
+12 RETURN
DC GND

AC GND   TWISTED PAIR   FRAME GND

FIGURE 9. INTERFACE CONNECTIONS

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4.1.1.1 Input Line Terminations

The SA400 has been provided with the capability of terminating the five input lines listed below.

1. Motor On
2. Direction Select
3. Step
4. Write Data
5. Write Gate

These lines are terminated through a 150 ohm resistor pack installed in a dip socket located at IC location 1E.

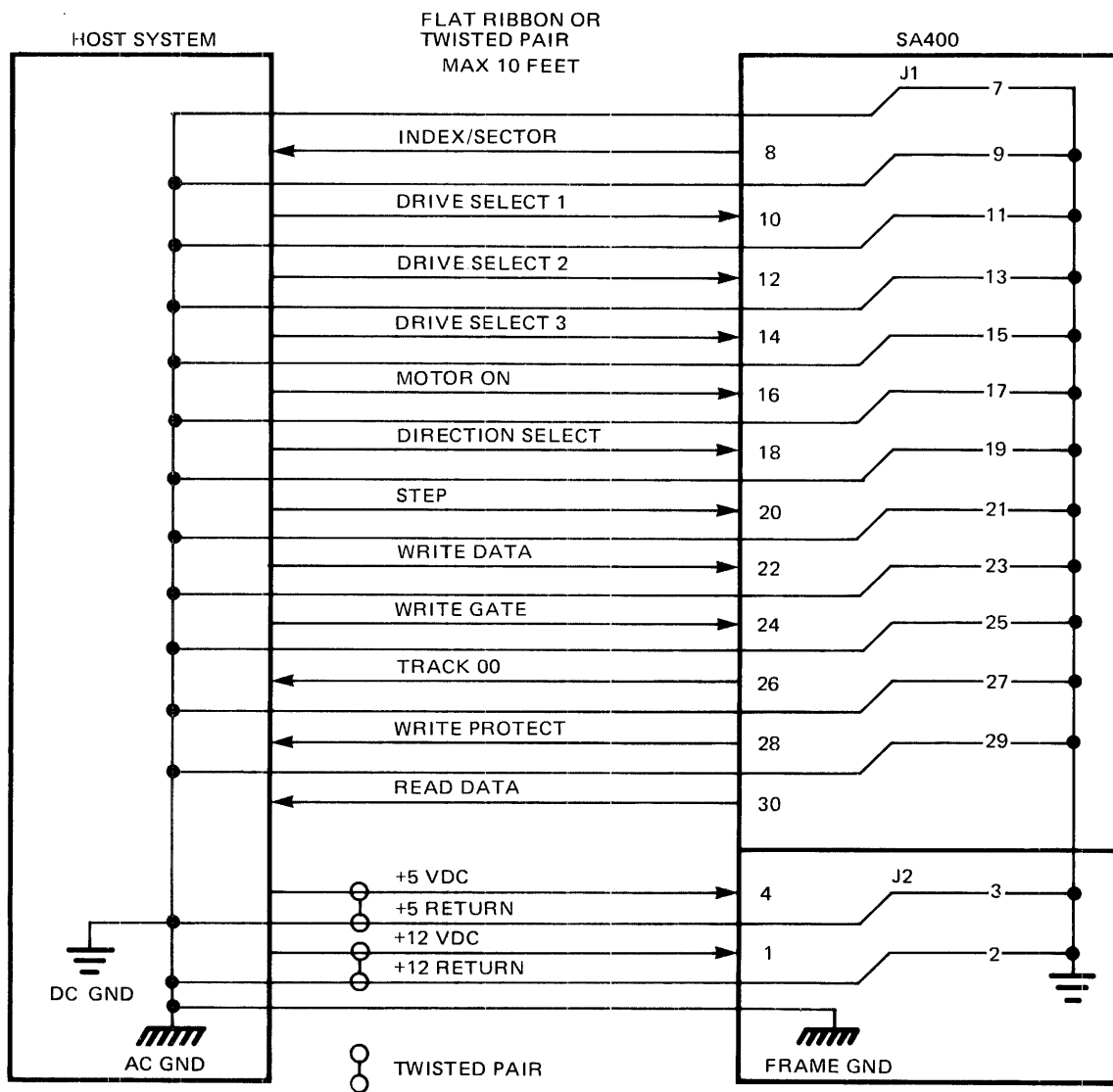In a single drive system this resistor pack should be kept in place to provide the proper terminations.

In a multiple drive system (Program Shunt position "MX" open) only the last drive on the interface is to be terminated. All other drives on the interface must have the resistor pack removed. External terminations may also be used, then the user must provide the terminations beyond the last drive and each of the five lines must be terminated to +5VDC through a 150 ohm ¼ watt resistor.

4.1.1.2 Drive Select 1-3

The SA400 as shipped from the factory is configured to operate in a single drive system. It can be easily modified by the user to operate with other drives in a multiplexed multiple drive system. The user can activate the multiplex option by cutting the "MX" position of the programmable shunt located in IC location 1F. This will allow the multiplexing of the I/O lines.

In a single drive system (program shunt position "MX" shorted), with program shunt position "HL" shorted, Drive Select when activated to a logical zero level, will load the R/W head against the diskette enabling contact of the R/W head against the media. Since "MX" is shorted, the I/O lines are always enabled.

In a multiple drive system (program shunt position "MX" open) the three input lines (Drive Select 1, Drive Select 2 and Drive Select 3) are provided so that the using system may select which drive on the interface is to be used. In this mode of operation only the drive with its Drive Select line active will respond to the input lines and gate the output lines. In addition, the selected drive will load its R/W head if program shunt position "HL" is shorted.

The program shunt, IC location 1F, positions "DS1", "DS2" and "DS3", are to be used to select which Drive Select line will active the I/O lines for a unique drive. As an example, if the user wants the first drive on the interface to be address 1, he must cut program shunt positions "DS2" and "DS3", and leave "DS1" intact.

The program shunt is AMP part number 435704-6. The shunt positions can be cut using AMP's tool part number 435705. The shunt is installed in a dip socket and at the user's option be removed and be replaced by a dip switch (AMP P/N 435626-4). The user may also choose to have the program shunts pre-programed and/or color coded by AMP. For this service contact your local AMP representative.

4.1.1.3 Motor On

This input when activated to a logical zero level will turn on the drive motor allowing reading or writing on the drive. A one (1) second delay after activating this line must be allowed before reading or writing. This line should be deactivated, for maximum motor life, if no commands have been issued to the drives within two seconds (10 revolutions of the media) after completion of a previous command.

As discussed in section 4.1.1.2, when program shunt position "HL" is shorted the R/W head will load when the Drive Select line is activated. A user selectable option is available where by the R/W head will load when the Motor On line is activated. This is accomplished by moving the program shunt over one position in its socket so position "MH" is shorted and position "HL" is open. With position "MH" shorted, the R/W head will load when the Motor On line is activated to a logical zero level.

4.1.1.4 Direction Select

This interface line is a control signal which defines direction of motion the R/W head will take when the Step line is pulsed. An open circuit or logical one defines the direction as "out" and if a pulse is applied to the Step line the R/W head will move away from the center of the disk. Conversely, if this input is shorted to ground or a logical zero level, the direction of motion is defined as "in" and if a pulse is applied to the step line, the R/W head will move towards the center of the disk.

4.1.1.5 Step

This interface line is a control signal which causes the R/W head to move with the direction of motion as defined by the Direction Select line.

The access motion is initiated on each logical zero to logical one transition, or the trailing edge of the signal pulse. Any change in the Direction Select line must be made at least $1\mu s$ before the trailing edge of the Step pulse. Direction Select logic level must be maintained $1\mu s$ after trailing edge of Step pulse. Refer to figure 3 for these timings.

4.1.1.6 Write Gate

The active state of this signal, or logical zero, enables Write Data to be written on the diskette. The inactive state, or logical one, enables the read data logic and stepper logic. Refer to figure 6 for timings.

4.1.1.7 Write Data (FM)

This interface line provides the data to be written on the diskette. Each transition from a logical one level to a logical zero level, will cause the current through the R/W head to be reversed thereby writing a data bit. This line is enabled by Write Gate being active. Refer to figure 7 for timings.

4.1.2 Output Lines

The output control lines have the following electrical specifications. Refer to figure 10 for the recommended circuit.

True = Logical Zero = Vout + 0.0V to + 0.4V
@ Iout = 48 ma (max)

False = Logical On = Vout + 2.5V to 5.25V (open collector @ Iout = 250 μa max)
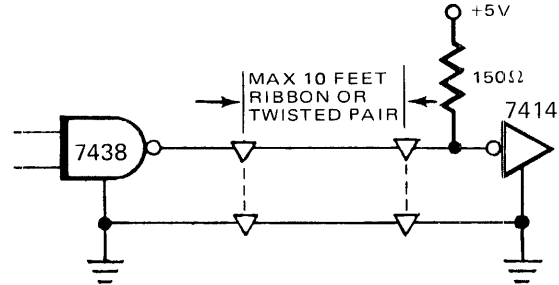
FIGURE 10. INTERFACE SIGNAL DRIVER/RECEIVER

4.1.2.1 Track 00

The active or logical zero state of this interface signal indicates when the drive's R/W head is positioned at track zero (the outermost track) and the access circuitry is driving current through phase "A" of the stepper motor. This signal is at a logical one level, or inactive state, when the
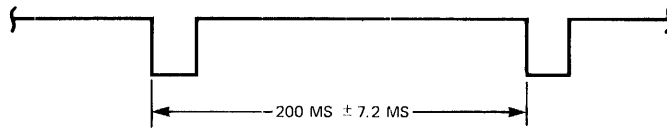
FIGURE 11. INDEX TIMING SOFT SECTORED (SA 104 MEDIA)
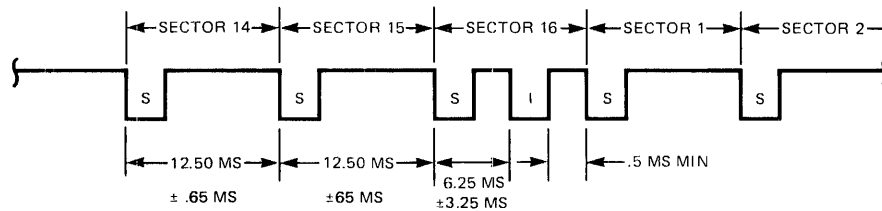
(SA105 MEDIA)
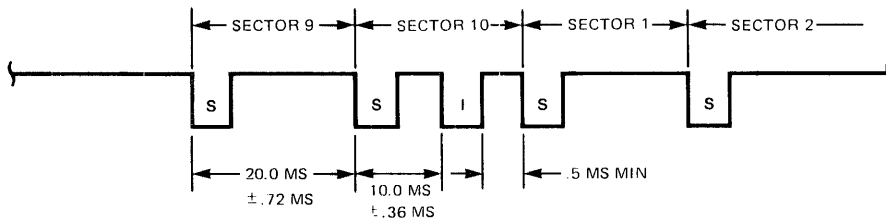
(SA107 MEDIA)

FIGURE 12. INDEX/SECTOR TIMING HARD SECTORED

drive's R/W head is not at track zero. When the drive's R/W head is at track zero and an additional step out pulse is issued to the drive, a mechanical stop will keep the R/W head at track zero but the Track 00 signal will go inactive. This is because the stepper motor will go to phase "C" and not phase "A". One more step out pulse will put the stepper motor back into phase "A" and the Track 00 signal will go active again.

4.1.2.2 Index/Sector

This interface signal is provided by the drive each time an index or sector hole is sensed at the Index/Sector photo detector. Normally, this signal is at a logical one level and makes the transition to the logical zero level each time a hole is sensed.

When using SA104 media (Soft Sectored), there will be one pulse on this interface signal per revolution of the diskette (200 ms). This pulse indicates the physical beginning of a track. Reference figure 11 for the timing.

When using SA105 or SA107 media (Hard Sectored), there will be 17 or 11 pulses on this interface line per revolution (200 ms). To indicate the beginning of a track, once per revolution there is one index transition between 16 or 10 equally spaced sector transitions. The timing for this signal is in figure 12. For recommended Index/Sector separator circuit, reference section 8.4.

When using the Index/Sector signal, look for an edge or transition rather than a level for determining its status. With no diskette inserted, this signal remains active or at a logical zero level which is an erroneous status.

4.1.2.3 Read Data

This interface line provides the "raw data" (clock and data together) as detected by the drive electronics. Normally, this signal is a logical one level and becomes a logical zero level for the active state. Reference figure 5 for the timing and bit shift tolerance within normal media variations.

4.1.2.4 Write Protect

This interface signal is provided by the drive to give the user an indication when a Write Protected Diskette is installed. The signal is logical zero level when it is protected. Under normal operation, the drive will inhibit writing with a protected diskette installed in addition to notifying the interface. If the "WP" trace is cut writing to the diskette is inhibited unless a Write Protect label is installed over the notch.

4.2 Power Interface

The SA400 requires only DC power for operation. DC power to the drive is provided via P2/J2 located on the non-component side of the PCB near the spindle drive motor. The two DC voltages, their specifications and their P2/J2 pin designators are outlined below. The specifications outlined on current requirements are for one drive. For multiple drive systems the current requirements are a multiple of the maximum current times the number of drives in the system.

4.2.1 Frame Ground

It is important that the drive be frame grounded to the host systems AC or frame ground. Failure to do so may result in drive noise susceptibility. Reference section 5.3 for the procedure.

P2 PIN	DC VOLTAGE	TOLERANCE	CURRENT	MAX RIPPLE (p to p)
1	+12 VDC	± 0.6 VDC	*1.80A MAX .90A TYP	100 mV max allowable
2	+12 Return			
3	+ 5 Return			
4	+ 5 VDC	± 0.25 VDC	.70A MAX .50A TYP	50 mV max allowable

*The 12 VDC current is composed of three components; head load current, diskette drive motor current, PCB functions and stepper motor. Each of these components has the following contribution to the 12 VDC current requirements.
  1. PCB functions and stepper motor (Drive "Standby" current): 0.4A TYP; 0.5A MAX
  2. Head Load (Drive Selected): 0.15A TYP; 0.2A MAX
  3. Drive Motor: Start (for 1 sec. max.)–1.0A TYP; 1.1A MAX
                 Running–0.35A TYP; 1.1A MAX (Motor Stalled)

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5.0 PHYSICAL INTERFACE

The electrical interface between the SA400 and the host system is via two connectors. The first connector, J1, provides the signal interface and the second connector, J2, provides the DC power.

This section describes the physical connectors used on the drive and the recommended connectors to be used with them. Refer to figure 15 for connector locations.

5.1 J1/P1 Connector

Connection to J1 is through a 34 pin PCB edge card connector. The dimensions for this connector are shown in figure 13. The pins are numbered 1 through 34 with the even numbered pins on the component side of the PCB and the odd numbered pins on the non-component side. Pin 2 is located on the end of the PCB connector closest to the corner and is labeled 2. A key slot is provided between pins 4 and 6 for optional connector keying.

The recommended connectors for P1 are tabulated below.

TYPE OF CABLE	MANUFACTURER	CONNECTOR P/N	CONTACT P/N
Twisted Pair, #26	AMP	583717-5	1-583616-1
Flat Cable	3M "Scotchflex"	3463-0001	NA
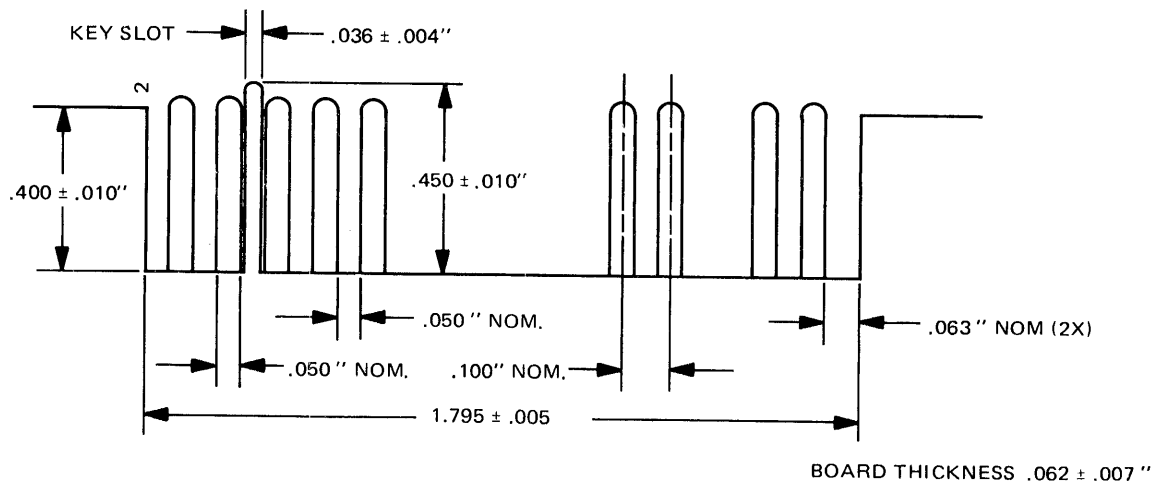
FIGURE 13. J1 CONNECTOR DIMENSIONS

5.2 J2/P2 Connector

The DC power connector, J2, is mounted on the non-component side of the PCB and is located near the spindle drive motor. J2 is a 4 pin AMP Mate-N-Lok connector P/N 350211-1. The recommended mating connector (P2) is AMP P/N 1-480424-0 utilizing AMP pins P/N 60619-1. J2, pin 1, is labeled on the component side of the PCB. Wire used should be #18 AWG. Figure 14 illustrates J2 connector as seen on the drive PCB from non-component side.

5.3 Frame Grounding

The SA400 must be frame grounded to the host system to insure proper operation. If the frame of
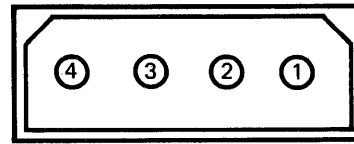
FIGURE 14. J2 CONNECTOR

the drive is not fastened directly to the frame of the host system with a good AC ground, a wire from the system AC frame ground must be connected to the SA400. For this purpose, a faston tab is provided on the drive near the motor control PCB where a faston connector can be attached or soldered. The tab is AMP P/N 61664-1 and its mating connector is AMP P/N 60972-1.
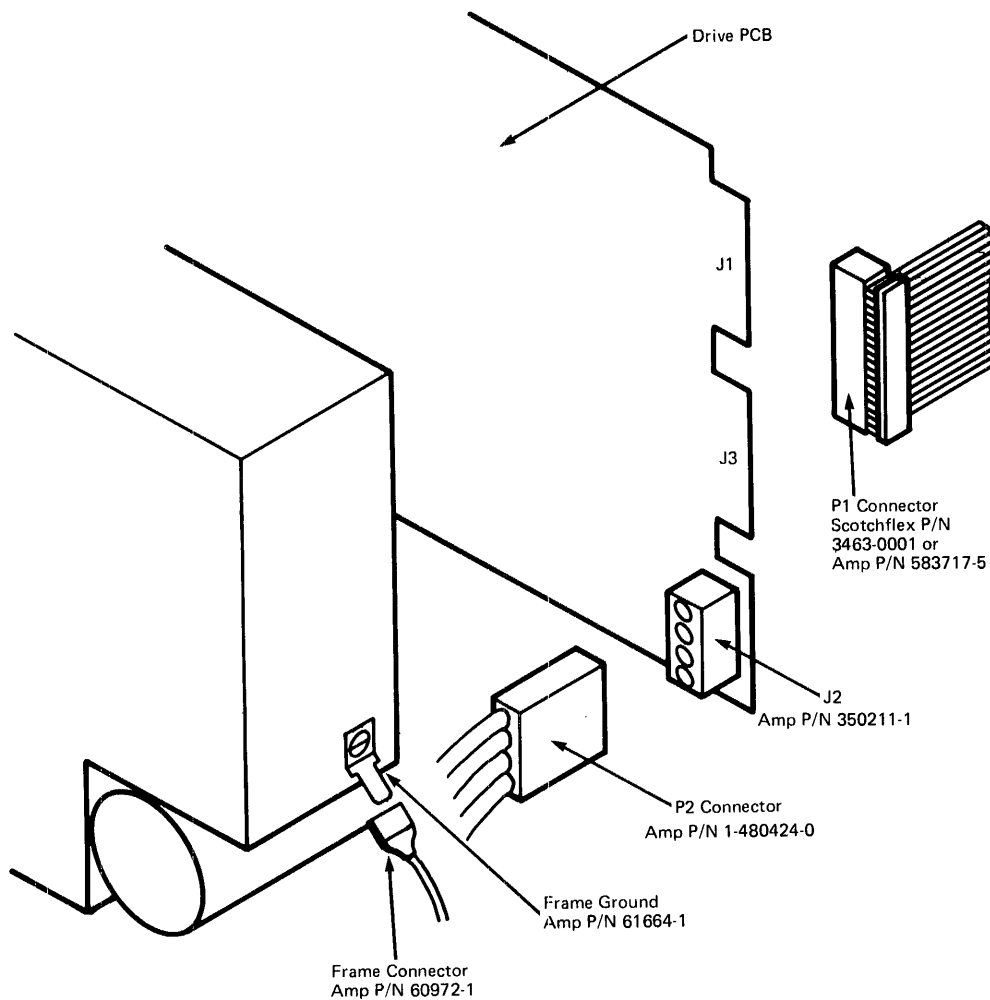
FIGURE 15. INTERFACE CONNECTORS—PHYSICAL LOCATIONS

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6.0 DRIVE PHYSICAL SPECIFICATIONS

This section contains the mechanical dimensions and mounting recommendations for the SA400.

6.1 Mechanical Dimensions

Reference figure 16 for dimensions of the SA400.

6.2 Mounting

As shipped from the factory, the SA400 is capable of being mounted in one of the following positions.

1. Top loading   — mounted upright.

2. Front loading   — mounted vertical with door opening left or right.

                                — mounted horizontal with PCB up. <u>Do not horizontal mount with PCB down</u>.

.06 ± .02 overhang

(.15 ± .05) typical

5.75 ± .03

(14.60 ± .07)

.86 ± .02 (4X)

(2.18 ± .05)

3.25 ± .03

(8.25 ± .07)

Mounting Holes: 4 on bottom, 2 on each side

#6-32 x .31 DP. (8X)

(.78)

8.00 max

(19.88)

.19 ± .01

(.48 ± .02)

.29 ± .02

(.73 ± .05)

5.50 ± .02

(13.97 ± .05)

3.12 ± .02 (8X)

(7.92 ± .05)

1.87 ± .02 (4X)

(4.74 ± .05)

FIGURE 16. SA400 DRIVE DIMENSIONS

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7.0 RECORDING FORMAT

The format of the data recorded on the diskette is totally a function of the host system. Data is recorded on the diskette using frequency modulation as the recording mode, i.e., each data bit recorded on the diskette has an associated clock bit recorded with it. Data written on and read back from the diskette takes the form as shown in figure 17. The binary data pattern shown represents a 101.
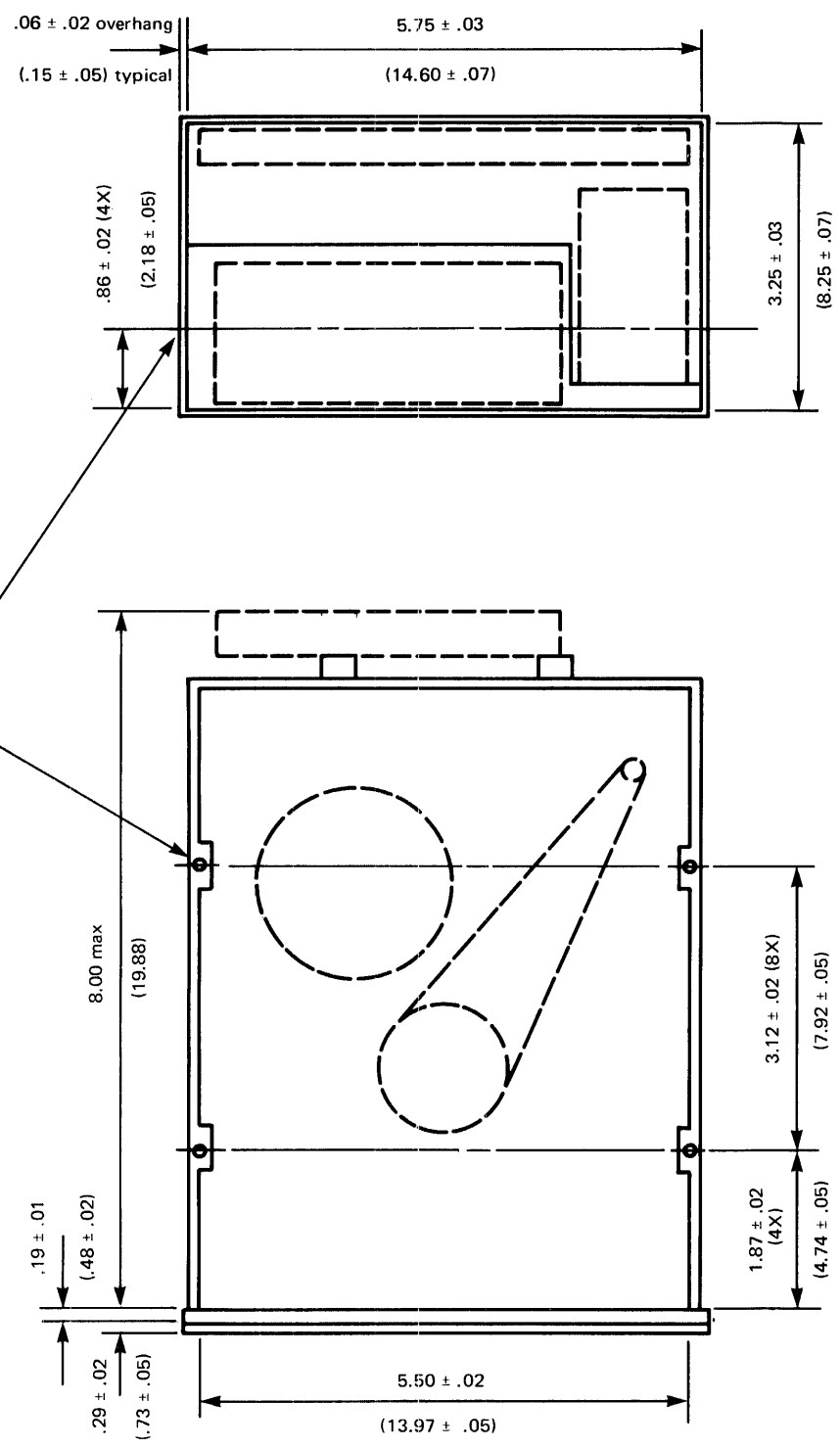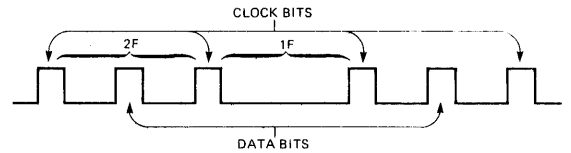

FIGURE 17. DATA PATTERN

7.1 Bit Cell

As shown in figure 18, the clock bits and data bits (if present) are interleaved. By definition, a Bit Cell is the period between the leading edge of one clock bit and the leading edge of the next clock bit.
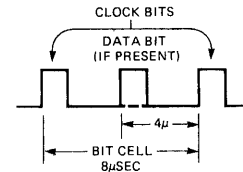
FIGURE 18. BIT CELL

7.2 Byte

A Byte, when referring to serial date (being written onto or read from the disk drive), is defined as eight (8) consecutive bit cells. The most significant bit cell is defined as bit cell 0 and the least significant bit cell is defined as bit cell 7. When reference is made to a specific data bit (i.e., data bit 3), it is with respect to the corresponding bit cell (bit cell 3).

During a write operation, bit cell 0 of each byte is transferred to the disk drive first with bit cell 7 being transferred last. Correspondingly, the most significant byte of data is transferred to the disk first and the least significant byte is transferred last.

When data is being read back from the drive, bit cell 0 of each byte will be transferred first with bit cell 7 last. As with reading, the most significant byte will be transferred first from the drive to the user.

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Figure 19 illustrates the relationship of the bits within a byte and figure 20 illustrates the relationship of the bytes for read and write data.

7.3 Track Format

Tracks may be formatted in numerous ways and is dependent on the using system. The SA400 can either use hard or soft sectored recording formats.

7.3.1 Soft Sectored Recording Format

In this format, the using system may record one long record or several smaller records. Each track is started by a physical index pulse and then each record is preceded by a unique recorded identifier. This type of recording is called soft sectoring.

Figure 21 shows the recommended soft sectored format. The format described is identical to the IBM format with the interrecord gaps G1, G2, G3 and G4 shortened. The SA104 minidiskette is the media to be used in soft sectoring.

7.3.1.1 Gaps

Each field on a track is separated from adjacent fields by a number of bytes. These areas are referred to as gaps and are provided to allow the updating of one field without affecting adjacent fields. At the end of each gap, except Gap 4, are four bytes of zeros which are used for synchronizing the data separator. As can be seen from figure 21, there are four different types of gaps on each track.

FIGURE 19. BYTE

BIT CELL 0 OF BYTE 0 IS FIRST DATA TO BE SENT TO THE DRIVE WHEN WRITING AND FROM THE DRIVE WHEN READING

BIT CELL 7 OF BYTE 17 IS LAST DATA TO BE SENT TO THE DRIVE WHEN WRITING AND FROM THE DRIVE WHEN READING
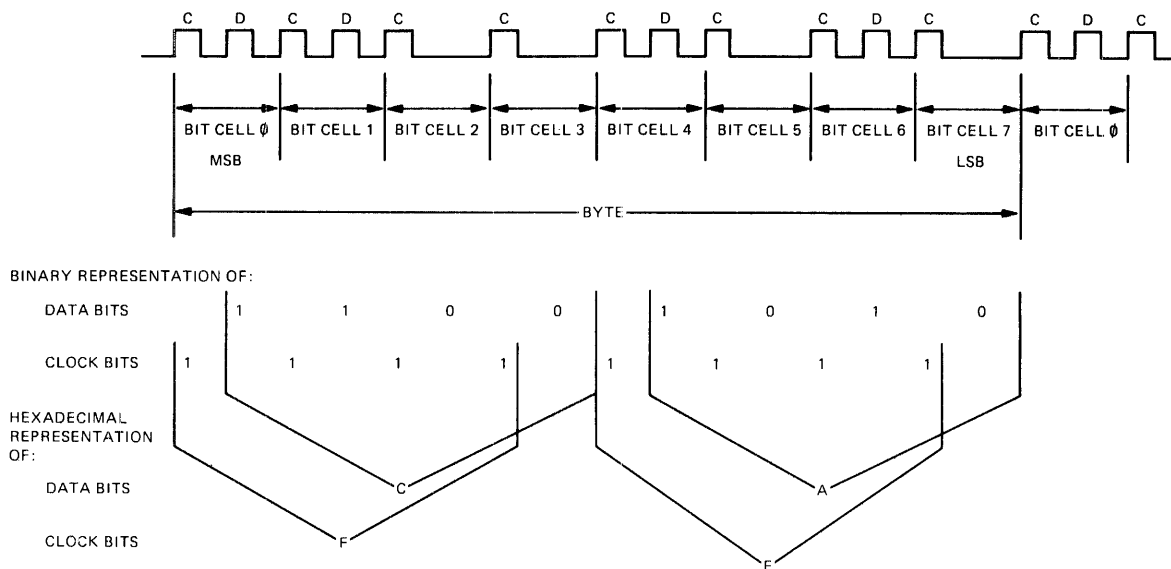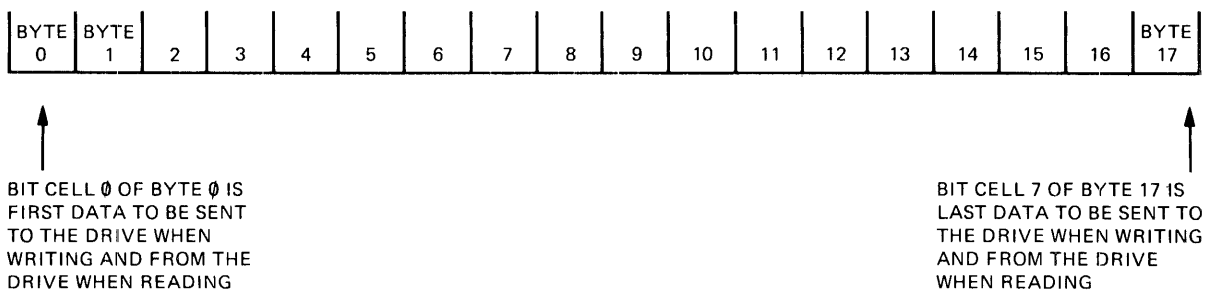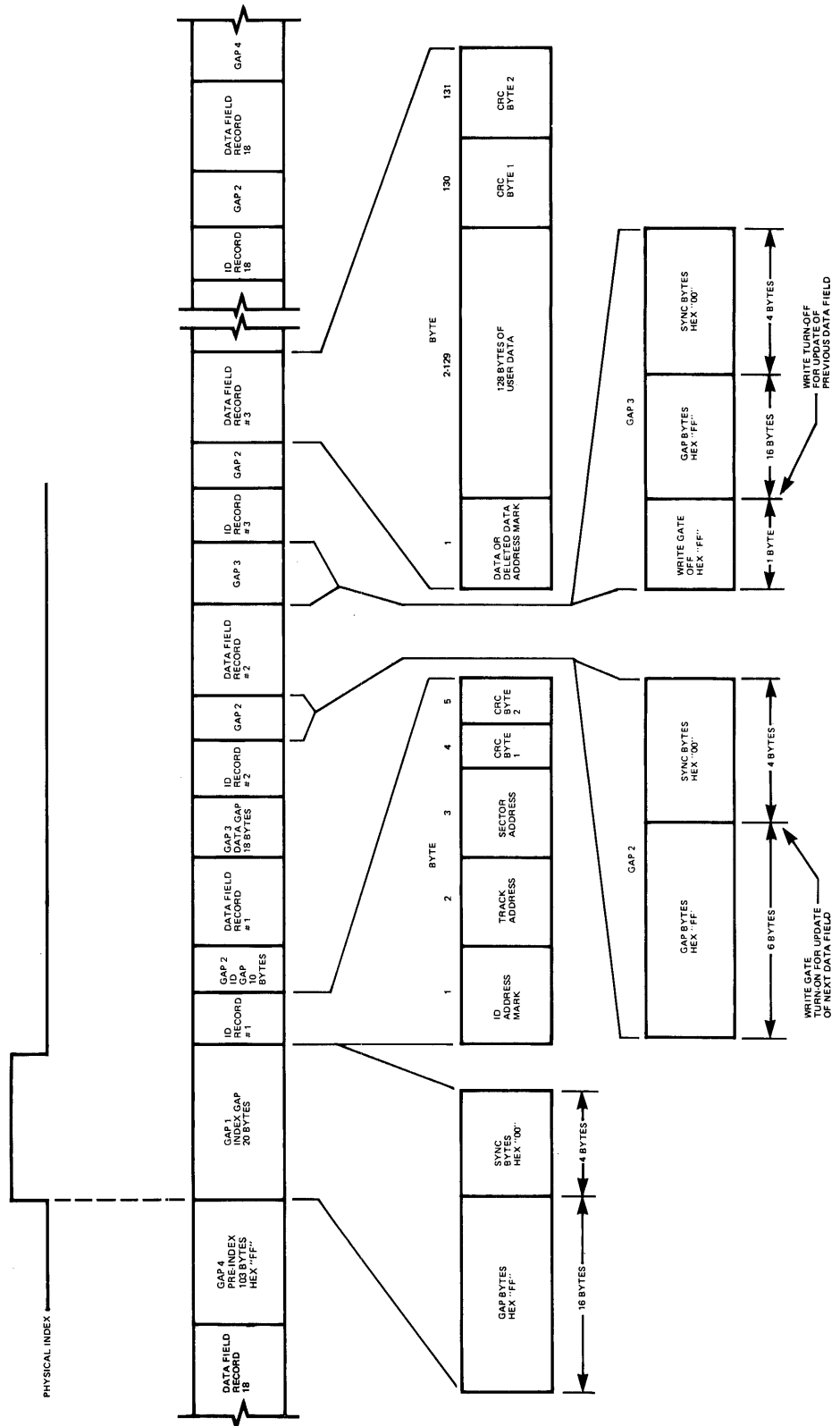
FIGURE 20. DATA BYTES

FIGURE 21. TRACK FORMAT-18 RECORD/TRACK

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Gap 1   Index Gap

This gap is defined as the 20 bytes between Pre-Index Gap and the ID Address Mark for Sector one. This gap is always 20 bytes in length and is not affected by any updating process.

Gap 2   ID Gap

The 10 bytes between the ID Field and the Data Field is defined as Gap 2 (ID Gap). This gap may vary in size slightly in length after the Data Field has been updated.

Gap 3   Data Gap

The 21 bytes between the Data Field and the next ID Field is defined as Gap 3 (Data Gap). As with the ID Gap, the Data Gap may vary slightly in length after the adjacent Data Field has been updated.

Gap 4   Pre-Index Gap

The 103 bytes between the last Data Field on a track and the Index Gap is defined as Gap 4 (Pre-Index Gap). Initially, this gap is nominally 116 bytes in length; however, due to write frequency tolerances and disc speed tolerances this gap may vary slightly in length. Also, after the data field of record 18 has been updated, this gap may again change slightly in length.

7.3.1.2   Address Marks (AM)

Address Marks are unique bit patterns one byte in length which are used in this recommended recording format to identify the beginning of ID and Data Fields and to synchronize the deserializing circuitry with the first byte of each field. Address Mark bytes are unique from all other data bytes in that certain bit cells do not contain a clock bit (all other data bytes have clock bits in every bit cell). There are three different types of Address Marks used. Each of these is used to identify different types of fields.

ID Address Mark

The ID Address Mark byte is located at the beginning of each ID Field on the diskette. The bit configuration for this Address Mark is shown in figure 22.

Data Address Mark

The Data Address Mark byte is located at the beginning of each normal Data Field on the diskette. The bit configuration for this Address Mark is shown in figure 23.

Deleted Data Address Mark

The Deleted Data Address Mark byte is located at the beginning of each Deleted Data Field on the diskette. The bit configuration for this Address Mark is shown in figure 24. This Address Mark can be used to flag special use Data Fields or other uses at the users option.
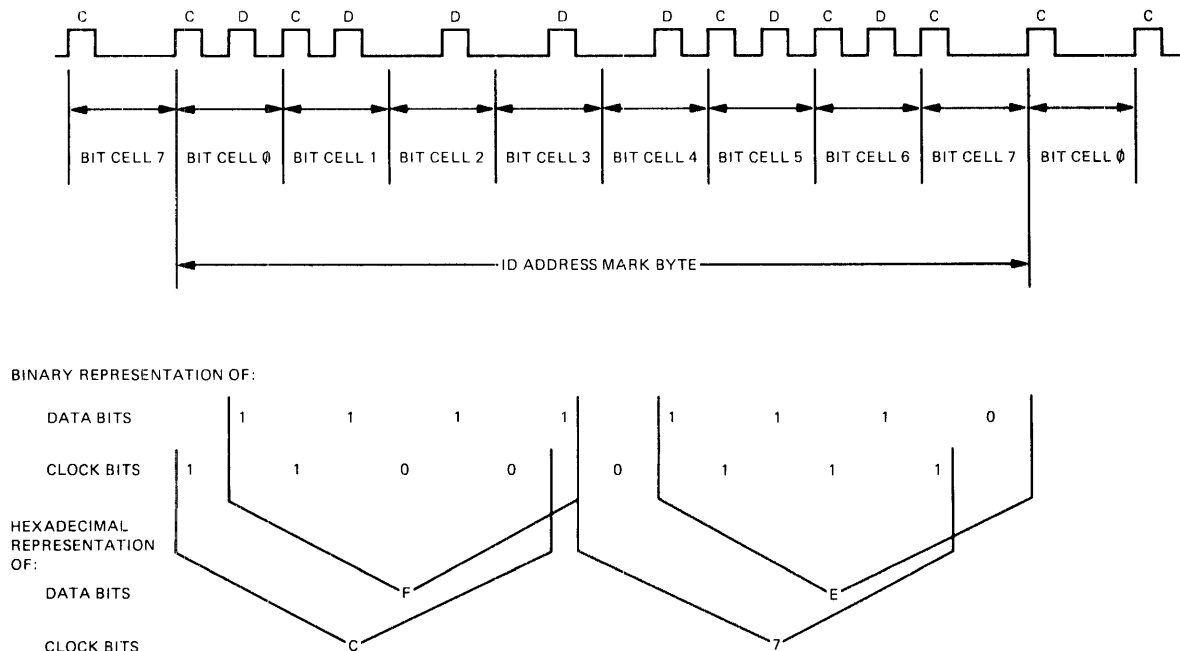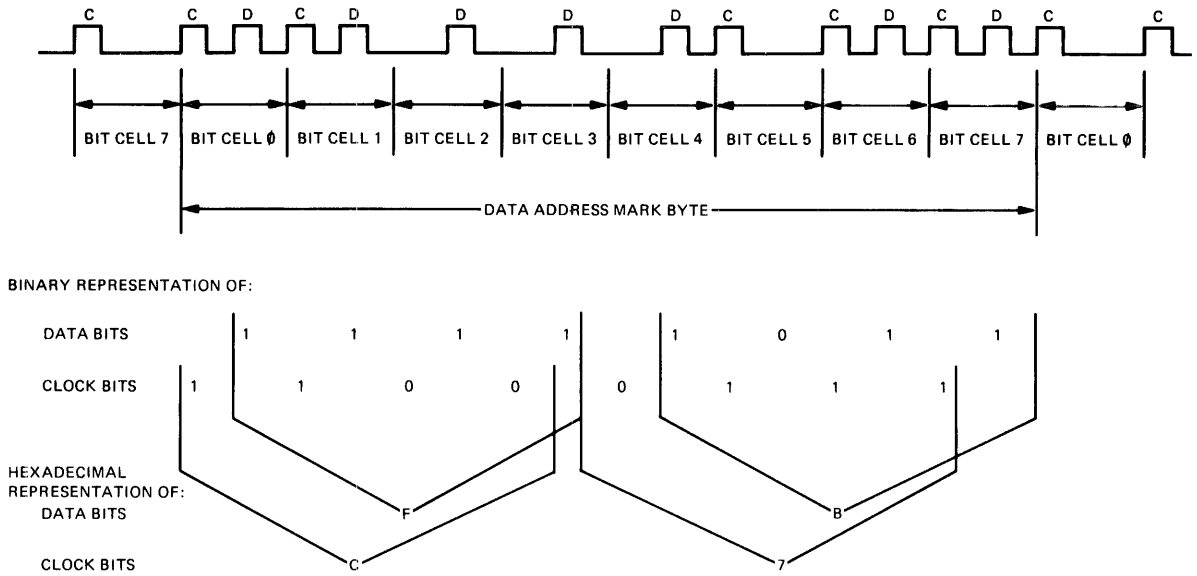
FIGURE 22.   ID ADDRESS MARK
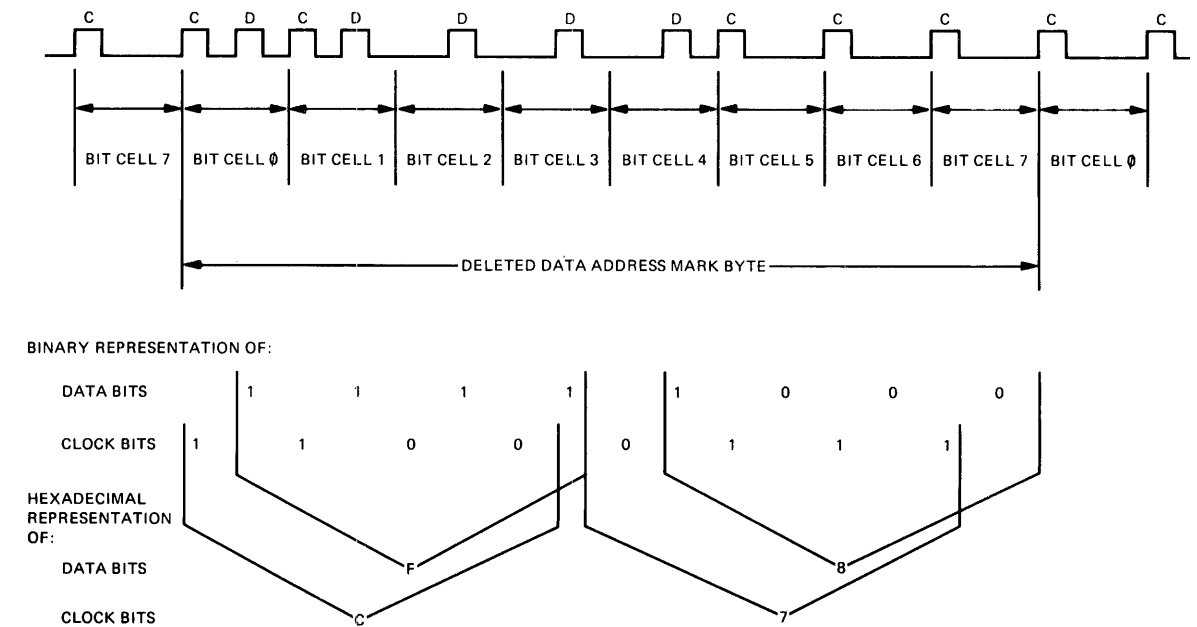
FIGURE 23. DATA ADDRESS MARK

FIGURE 24. DELETED DATA ADDRESS MARK

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7.3.1.3 CRC

Each field written on the diskette is appended with two Cyclic Redundancy Check (CRC) bytes. These two CRC bytes are generated from a cyclic permutation of the data bits starting with bit zero of the address mark and ending with bit seven of the last byte within a field (excluding the CRC bytes). When a field is read back from a diskette, the data bits (from bit zero of the address mark to bit seven of the second CRC byte) are divided by the same generator polynomial. A non-zero remainder indicates an error within the data read back from the drive while a remainder of zero indicates the data has been read back correctly from the disk. Reference section 8.0 for recommended circuitry.

7.3.1.4 Optional Soft Sectored Formats

Figure 25 contains optimized formats for one sector per track to 18 sectors per track. All drive tolerances have been taken into account in developing these formats. For any other formats, please contact the factory.

7.3.2 Hard Sectored Recording Format

In this format, the using system may record up to 16 or 10 sectors (records) per track. Each track is started by a physical index pulse and each sector is started by a physical sector pulse. This type of recording is called hard sectoring. Figure 26 illustrates the hard sectored formats. The SA105 or SA107 minidiskette is to be used for these formats. All drive tolerances have been taken into account in developing these formats.
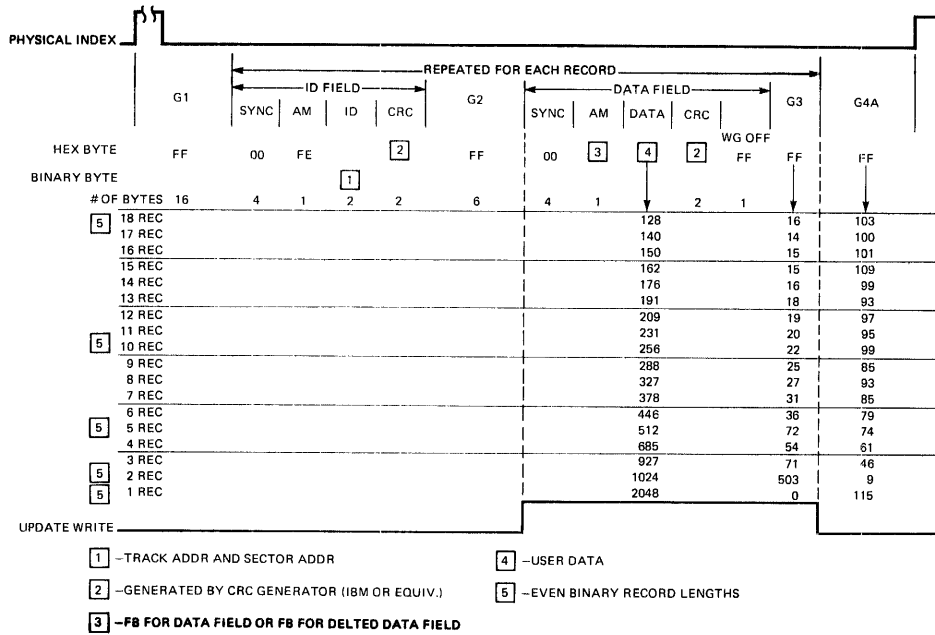

	G1	ID FIELD				G2	DATA FIELD				G3	G4A
		SYNC	AM	ID	CRC		SYNC	AM	DATA	CRC		
HEX BYTE	FF	00	FE		[2]	FF	00	[3]	[4]	[2]	WG OFF FF	FF	FF
BINARY BYTE				[1]									
# OF BYTES	16	4	1	2	2	6	4	1		2	1		

	DATA	G3	G4A
[5] 18 REC	128	16	103
17 REC	140	14	100
16 REC	150	15	101
15 REC	162	15	109
14 REC	176	16	99
13 REC	191	18	93
12 REC	209	19	97
11 REC	231	20	95
[5] 10 REC	256	22	99
9 REC	288	25	85
8 REC	327	27	93
7 REC	378	31	85
6 REC	446	36	79
[5] 5 REC	512	72	74
4 REC	685	54	61
3 REC	927	71	46
[5] 2 REC	1024	503	9
[5] 1 REC	2048	0	115

[1] –TRACK ADDR AND SECTOR ADDR

[2] –GENERATED BY CRC GENERATOR (IBM OR EQUIV.)

[3] –F8 FOR DATA FIELD OR FB FOR DELTED DATA FIELD

[4] –USER DATA

[5] –EVEN BINARY RECORD LENGTHS

FIGURE 25. SOFT SECTORED FORMATS

SECTOR SEPARATION DONE BY THE USING SYSTEM
FM RECOMMENDED FORMAT

	G1	ID	DATA FIELD	CRC	G2
HEX BYTE	HEX 00	HEX FB	[1]	[2]	HEX FF
# OF BYTES	16	1		2	

	DATA FIELD [1]	G2
16 SECTORS	128	48
8 SECTORS	256	115
4 SECTORS	512	250
2 SECTORS	1024	519
1 SECTORS	2048	1058

[1] –USER DATA

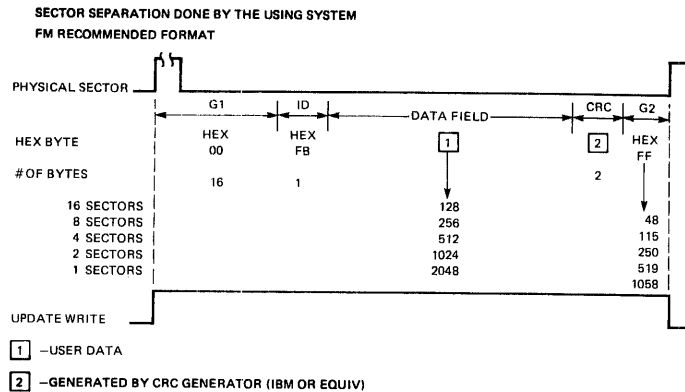[2] –GENERATED BY CRC GENERATOR (IBM OR EQUIV)

FIGURE 26. HARD SECTORED FORMATS

8.0 APPLICATION NOTES

This section contains recommended circuits for data separation, AM detection, CRC generation, Index/Sector separation and ready circuit. It also contains applicable timing charts where required.

8.1 Data Separator

The data separator is a two time constant separator, that is, the clock and data pulses must fall within pre-specified time frames or windows. The clock and data windows are developed in the data separation circuit. Figure 27 shows the functional diagram and figure 28 shows the timing diagram of the circuit.

Two data windows are supplied. The short window, 5.9 μs, is used when the previous bit cell had a data pulse in it. The long window, 6.0 μs, is used when the previous bit cell had no data pulse.

If the data pulse initially falls in the data window, -Separated Data is sent back to the OR block that generates the data window to assure that the full data pulse is allowed through before the window falls.

The clock window will take up the remainder of the bit cell time, either 2.1 μs or 2 μs.

In discussing the data separator circuit, figure 27, initially assume all circuits are reset (inactive) and that the +READ DATA line contains what is shown in figure 28.

With both SS1 and SS2 off, +Clk Window is active. The first Read Data pulse will be allowed through AND A2 and out as -Sep. Clk. -Sep. Clk. is sent out onto the interface line and to L1, SS1 and SS2. Since FF1 is off, SS1 will be held reset. The -Sep. Clk. pulse will trigger SS2. The output of SS2 is sent to the OR block which in turn becomes +Data Window enabling AND A1. The next pulse on +Read Data will be allowed through A1 becoming -Separated Data. -Separated Data sets L1 which in turn enables FF1. FF1 is clocked on by SS2 timing out (6.0 μs) and +Clk Window becoming active. The Q output of FF1 will hold SS2 reset and allow SS1 to trigger with receipt of the next clock pulse.

The next clock pulse, bit cell 1, is anded with +Clk Window and becomes the next -Sep. Clk. -Sep. Clk. will reset L1 and Trigger SS1 on. When SS1 becomes active, +Data Window becomes active enabling AND A1. Since bit cell 1 has no data bit it in, L1 will remain reset which will enable FF1 to
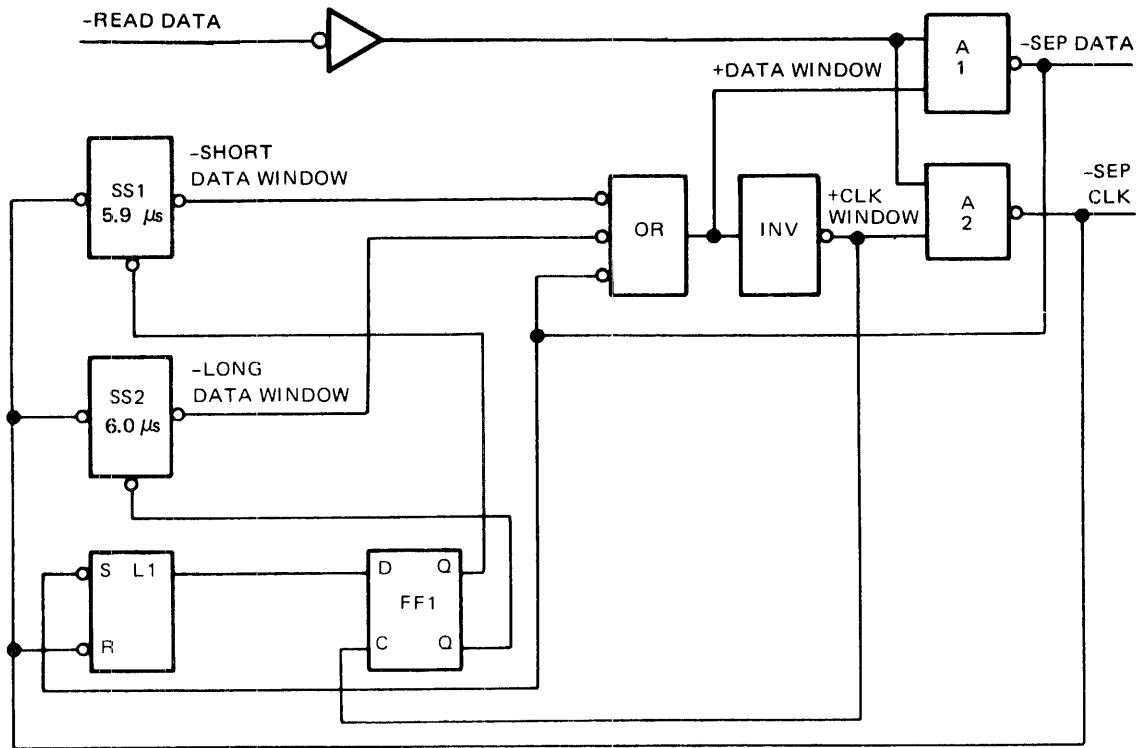
27

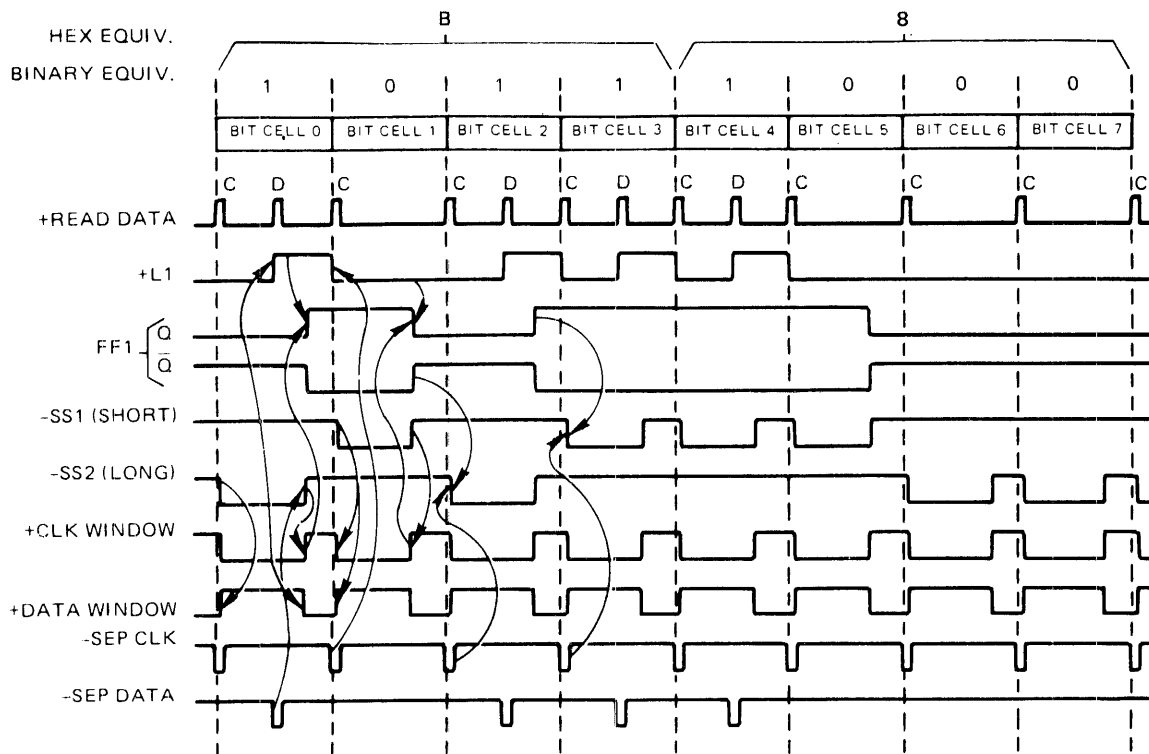**FIGURE 27. DATA SEPARATOR FUNCTIONAL DIAGRAM**

FIGURE 28. DATA SEPARATOR TIMING DIAGRAM

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be clocked off when +Data Window falls (5.9 μs). When FF1 is clocked off the Q output will hold SS1 reset and allow SS2 to be triggered.

The next clock pulse, bit cell 2, is anded with +Clk Window and becomes -Sep. Clk. -Sep. Clk. will further reset L1, which was off, and trigger SS2 on. When SS2 becomes active, -Long Data Window, and enables AND A1 allowing the data pulse in bit cell 2 to become -Sep Data. -Sep Data will set L1 which enables FF1 to be clocked on when +Data Window falls. When +Data Window falls, the Q output will hold SS2 reset and allow SS1 to trigger.

This procedure continues until the using system terminates the Read Operation.

When using this data separator with the soft sectored format described in section 7.4.1, the user should be aware that the data separator will get out of sync during the Address Mark bytes. This is due to the missing clock bits in bit cells 2, 3 and 4. The circuit discussion in section 8.2, Read Data circuits, will describe how to recover from this.

8.1.1 True FM Data Separator

The circuit illustrated in figure 29 is a true data separator, that is, it will stay in sync through the address mark. The data separator discussed in section 8.1 will get out of sync in the AM byte. The circuit should be used as the data separartor for the single chip controllers.

8.2 Read Data Circuits

The purpose of the following is to provide an example of specific circuitry for interfacing the SA400 to enable reading data in the soft sectored format and using the data separator of paragraph 8.1. Figures 30, 31 and 32 illustrate. When a read operation is required, the host system selects the desired drive and keeps the Write Gate inactive. After the drive is selected, read data pulses are issued to the host system.

Sixteen bits of all zero's followed by a pattern of missing clock and data bits (an address mark) identify the start of a field. A missing clock after a data bit sequence of 1, 1, 1 is common to all address marks and is used to enable the bit ring to sequence. The clock bit pattern is shifted into the clock register, the data bit pattern is shifted into the data register and during bit ring 7, the AM detected latch is set if the accumulated clock and

data patterns correspond exactly to that of an address mark. If not address mark is detected, the CRC register and synchronization circuitry is reset during the bit ring 7.

A one's catching latch is used to detect a pulse on the separated data line (from the diskette drive) and the leading edge of the separated clock line (from the diskette drive) is used to shift the state of the latch into a shift register. The trailing edge of the separated clock line is used to reset the one's catching latch.

The missing clock bit of an address mark causes the data separator in the drive to shift out of phase so that the data bit pattern is placed onto the separated clock line (see figure 30) until a missing data bit occurs to shift the data separator back to clock bits on the separated clock line. During the out of phase sequence, clock bits are detected by the one's catching latch rather than data bits.
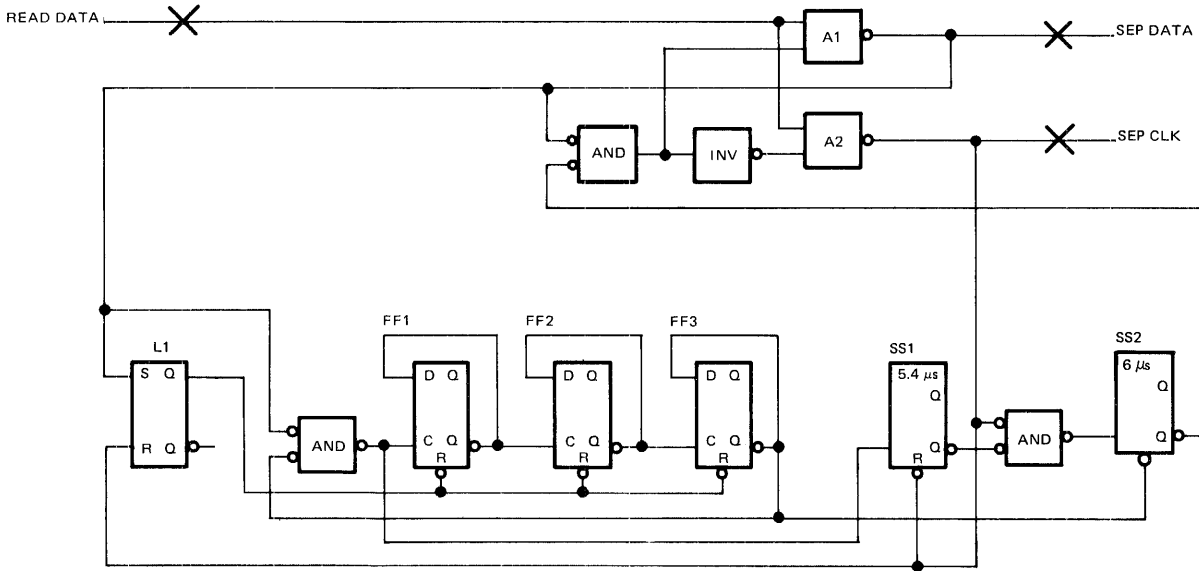
The out of phase condition is detected and the appropriate multiplexing of the separated data is performed to shift the recorded clock bits into the clock register and the recorded data bits into the data register so that the address mark patterns can be detected.

A 100 nsec single shot is triggered when a missed separated clock is detected. This pulse is used in place of the missed clock pulse to shift the bit from the one's catching latch into the shift register. The phase shift of the data separator causes the bit following the missed bit to become the separated clock, therefore a one bit is shifted into its register, and a zero is shifted into the other register corresponding to the missed bit.

In the example circuitry clock and data bits are shifted into two separate registers. The address mark detection consists simply of identification of the unique clock and data patterns read from the drive. This identification is accomplished by the logical "and" of the appropriate clock and data bits (see figure 31 of the example read circuitry).

8.3 CRC Generating and Checking Circuitry

Each field written on the diskette is appended with two Cyclic Redundancy Check (CRC) bytes. These two CRC bytes are generated from a cyclic permutation of the data bits starting with bit zero of the address mark and ending with bit seven of the last byte within a field (excluding the CRC bytes). This cyclic permutation is the remainder from the division of the data bits in the field

READ DATA   ✕   ━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━ A1 ━━━━━━ ✕ .SEP DATA

AND   INV   A2 ━━━━━ ✕ .SEP CLK

L1   FF1   FF2   FF3   SS1   SS2

| S Q | | D Q | | D Q | | D Q | | 5.4 μs Q | | 6 μs Q |
| R Q | AND | C Q R | | C Q R | | C Q R | | R | AND | Q |

NOTE: SINGLE SHOT TIMES INCLUDES THE DATA BIT PULSE WIDTH.

TIMING DIAGRAM

━GAP 2━   ━DATA AM━   ━DATA

C   C   C   C D C D   D   D   D C   C D C D C   C

READ DATA
SEP DATA
SEP CLK
L1
SS1
FF1
FF2
FF3
SS2
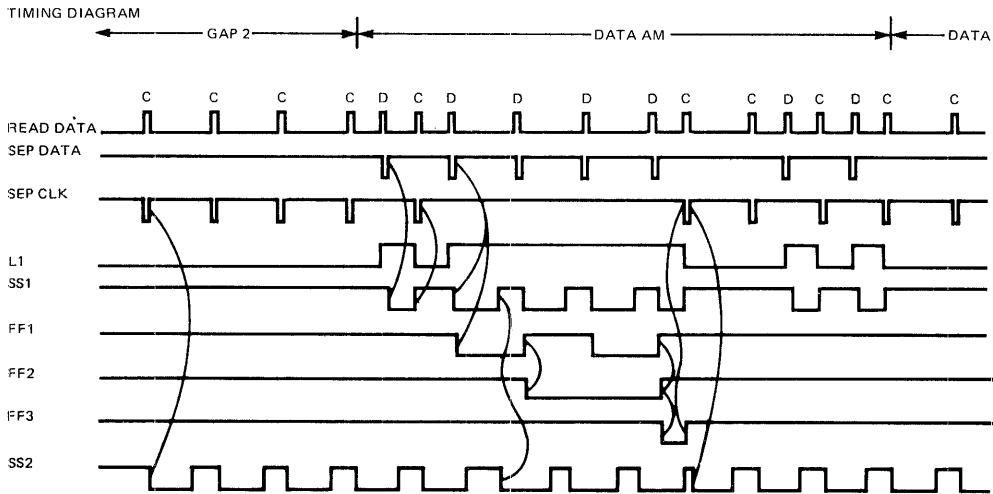
FIGURE 29. TRUE DATA SEPARATOR

30
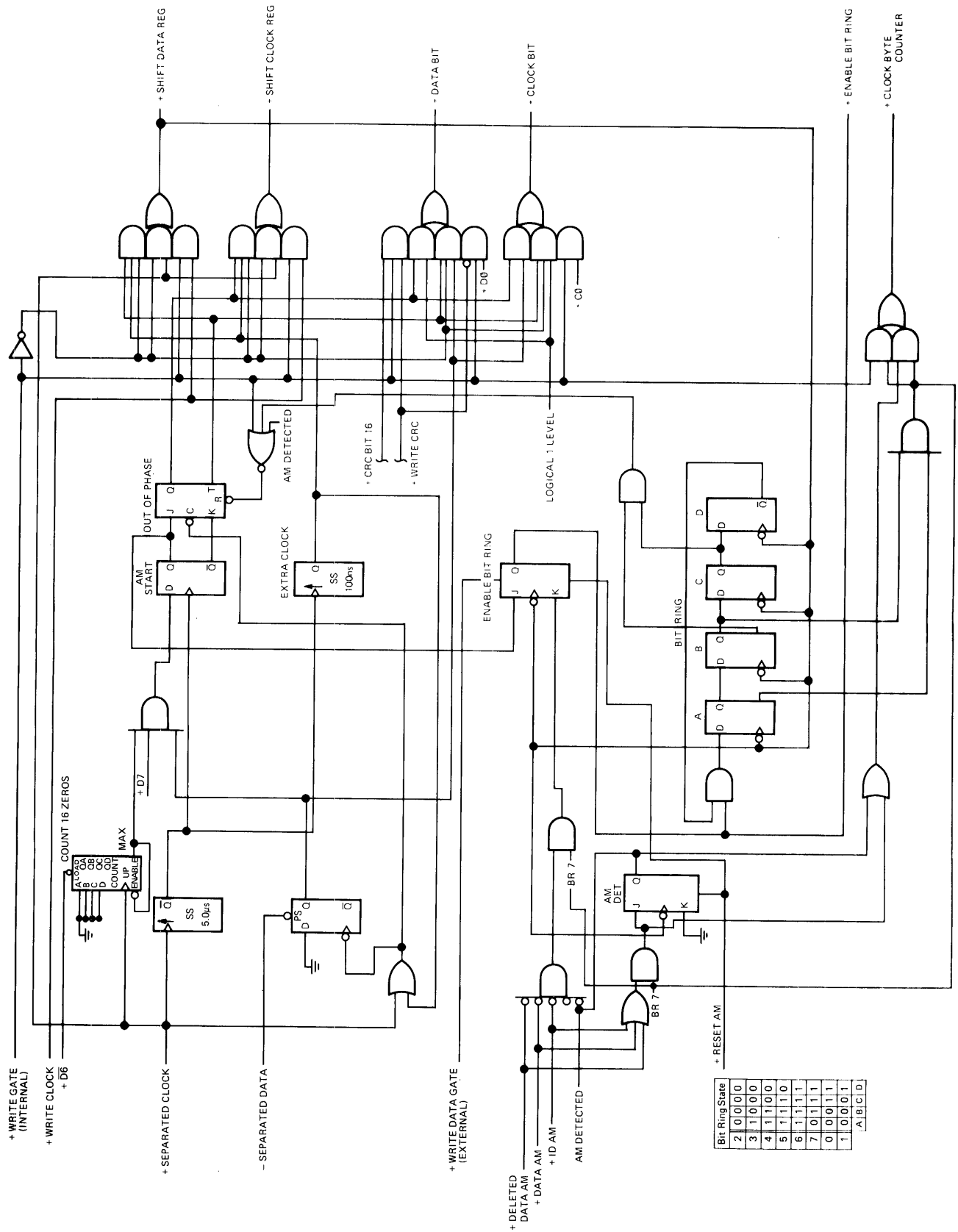
FIGURE 30. REGISTER CONTROLS AND AM DETECTION

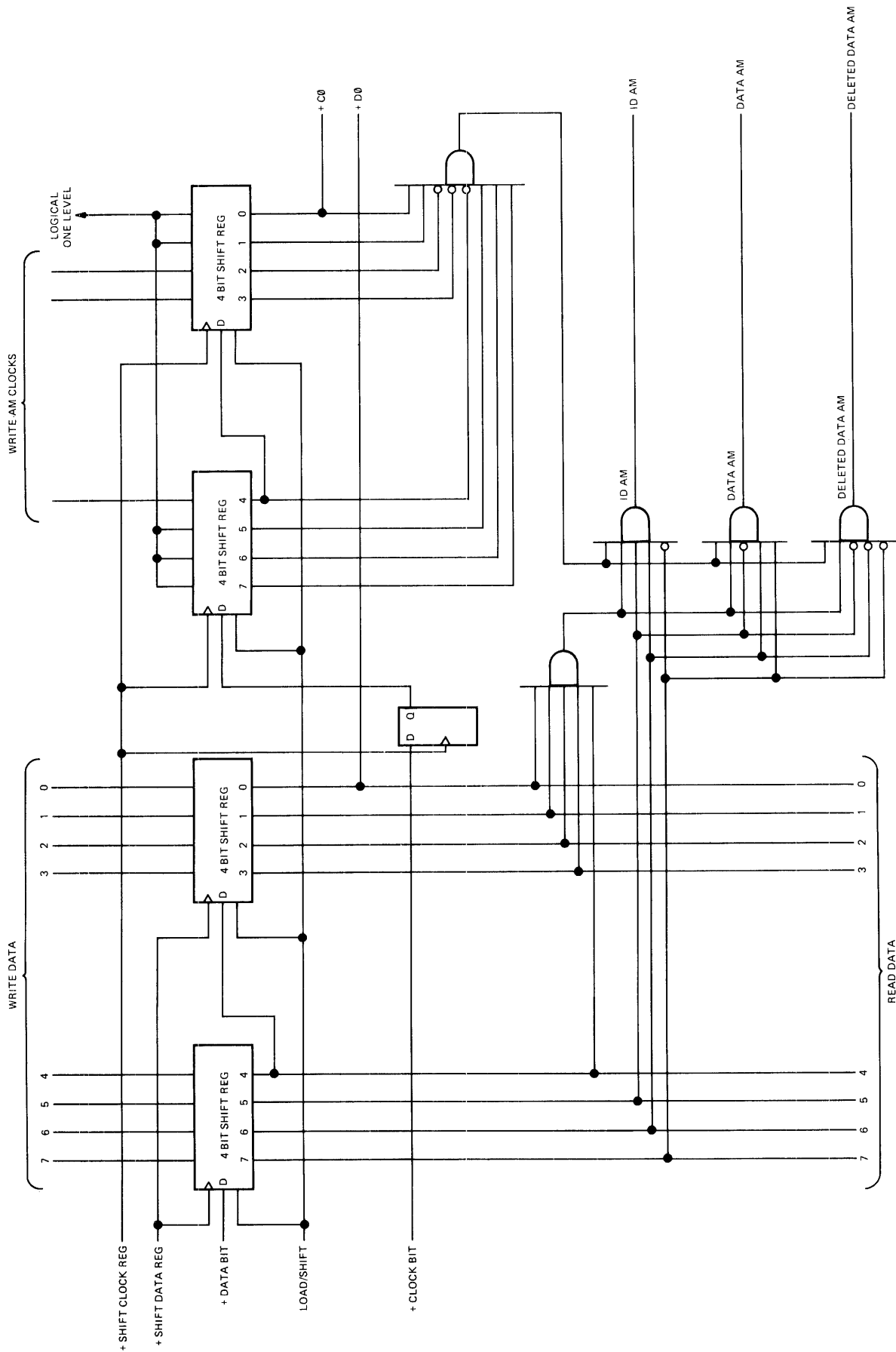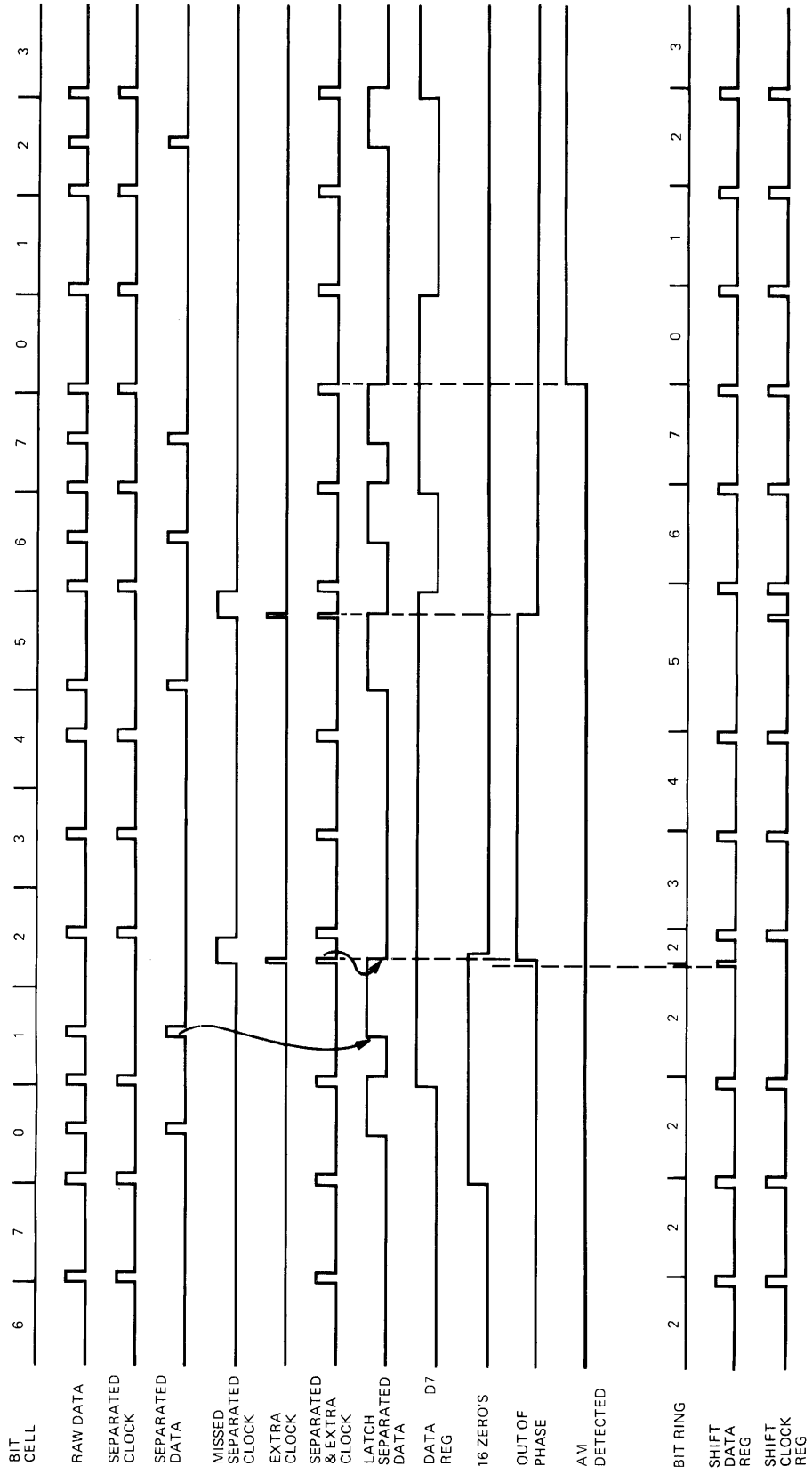| Bit Ring State				
2	0	0	0	0
3	1	0	0	0
4	1	1	0	0
5	1	1	1	0
6	1	1	1	1
7	0	1	1	1
7	0	0	1	1
1	0	0	0	1
	A	B	C	D

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FIGURE 31. DATA AND CLOCK REGISTERS

FIGURE 32. AM TIMING

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(represented as an algebraic polynomial) by a generator polynomial G(X). For all fields recorded on the diskette, this generator polynomial is:

$$G(X) = X^{16} + X^{12} + X^5 + 1.$$

When a field is read back from a minidiskette, the data bits (from bit zero of the address mark to bit seven of the second CRC byte) are divided by the same generator polynomial G(X) and a non-zero remainder indicates an error within the data read back from the drive while a remainder of zero indicates the data has been read back correctly from the disc or an undetectable error has been read back.

The necessary division described above can be accomplished by the use of relatively simple logic circuitry. Figure 33 shows the basic circuitry to both generate and check data using the generator polynomial G(X). In order to avoid CRC bytes of all zeros, all of the flip-flops in the logic diagram are preset to ones prior to the data being shifted through the circuit.

Figure 33 of the example read circuitry illustrates the circuitry necessary for both generating and checking the CRC. For both generating and checking the CRC circuitry starts processing data with the data bit in bit cell 2 of the address mark.

Generation of the CRC is completed by shifting zeros into the input of the CRC circuitry and using the CRC Write Data as the data to be written on the disc.

Checking of the CRC is completed by sampling the output of the Data Correct line during bit cell 0 of the first byte of the gap following the second CRC character.

Single chip CRC generators are currently available. They are the Fairchild 9401 and the Motorola 8501.

8.4   Index/Sector and Ready Logic

Figures 34 and 35 illustrate the recommended Index/Sector separator and Ready Logic. The logic requires 3 Index/Sector transitions after Drive Select before allowing Index Detect. It does not allow for a false Index Detection if Drive Select goes active between Sector 16 or 10 and Index.

Drive Select to Ready delay is less than 60 ms and greater than 40 ms if the diskette is within 80% of speed. The Ready will go inactive at the loss of either Drive Select or 15 or 24 ms after the diskette drops below 80% of speed.

8.5   Error Detection and Correction

8.5.1 Write Error

If an error occurs during a write operation, it will be detected on the next revolution by doing a read operation, commonly called a "write check." To correct the error, another write and write check operation must be done. If the write operation is not successful after ten (10) attempts have been made, a read operation should be attempted on another track to determine if the media or the drive is failing. If the error still persists, the disk should be considered defective and discarded.

8.5.2 Read Error

Most errors that occur will be "soft" errors; that is, by performing an error recovery procedure the data will be recovered.

Soft errors are usually caused by:

1. Airborne contaminants that pass between the read/write head and the disk. These contaminants will generally be removed by the cartridge self-cleaning wiper.

2. Random electrical noise which usually lasts for a few μ sec.

3. Small defects in the written data and/or track not detected during the write operation which may cause a soft error during a read.

The following procedures are recommended to recover from the above mentioned soft errors:

1. Reread the track ten (10) times or until such time as the data is recovered.

2. If data is not recovered after using step 1, access the head to the adjacent track in the same direction previously moved, then return to the desired track.

3. Repeat step 1.

4. If data is not recovered, the error is not recoverable.

8.5.3 Seek Error

Seek errors are detected by reading an ID field after the seek is completed. The ID field contains the track address. If a seek error is detected, the host system should issue a recalibrate operation (step out until Track 00 line goes active) and seek back to the original track.
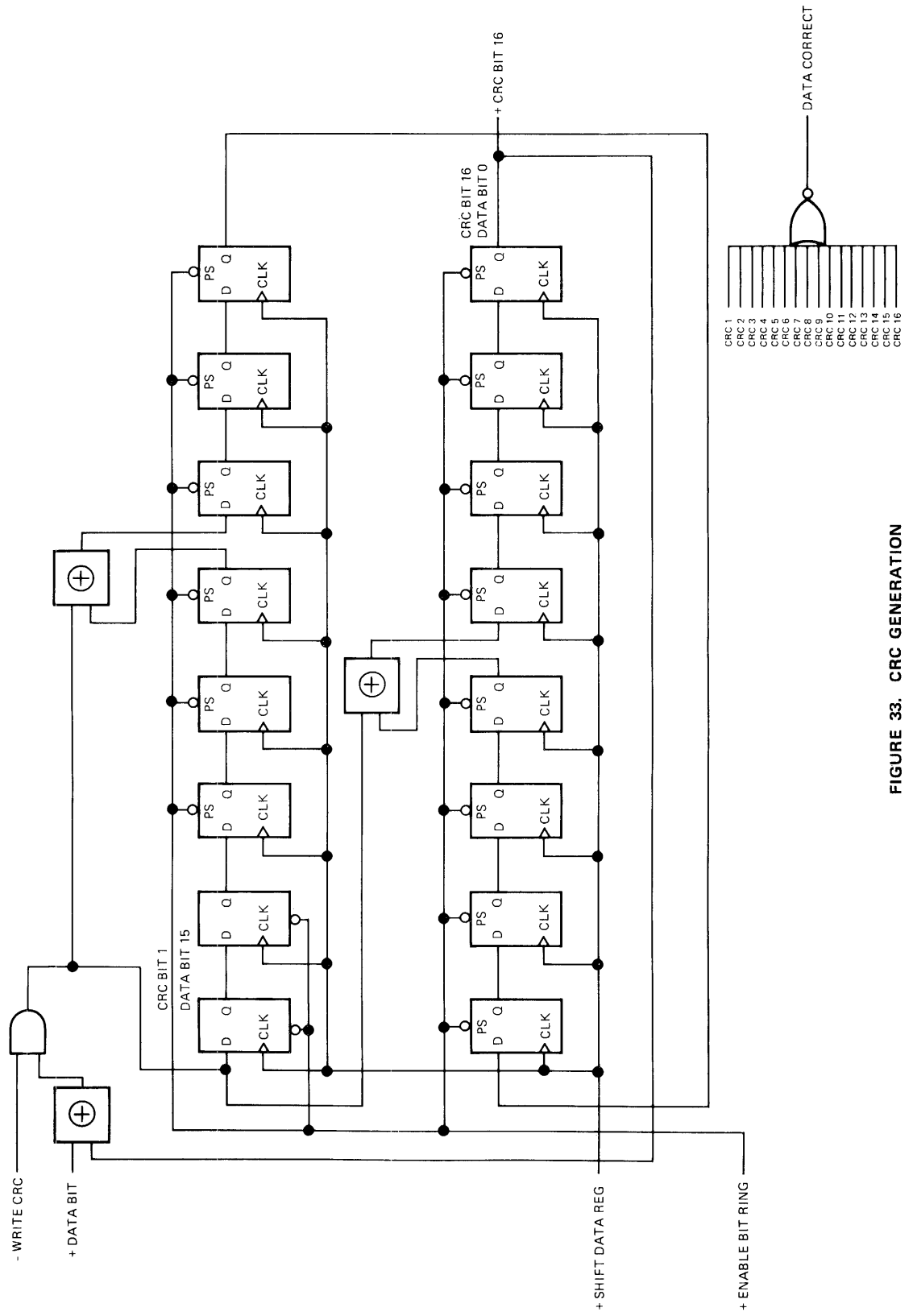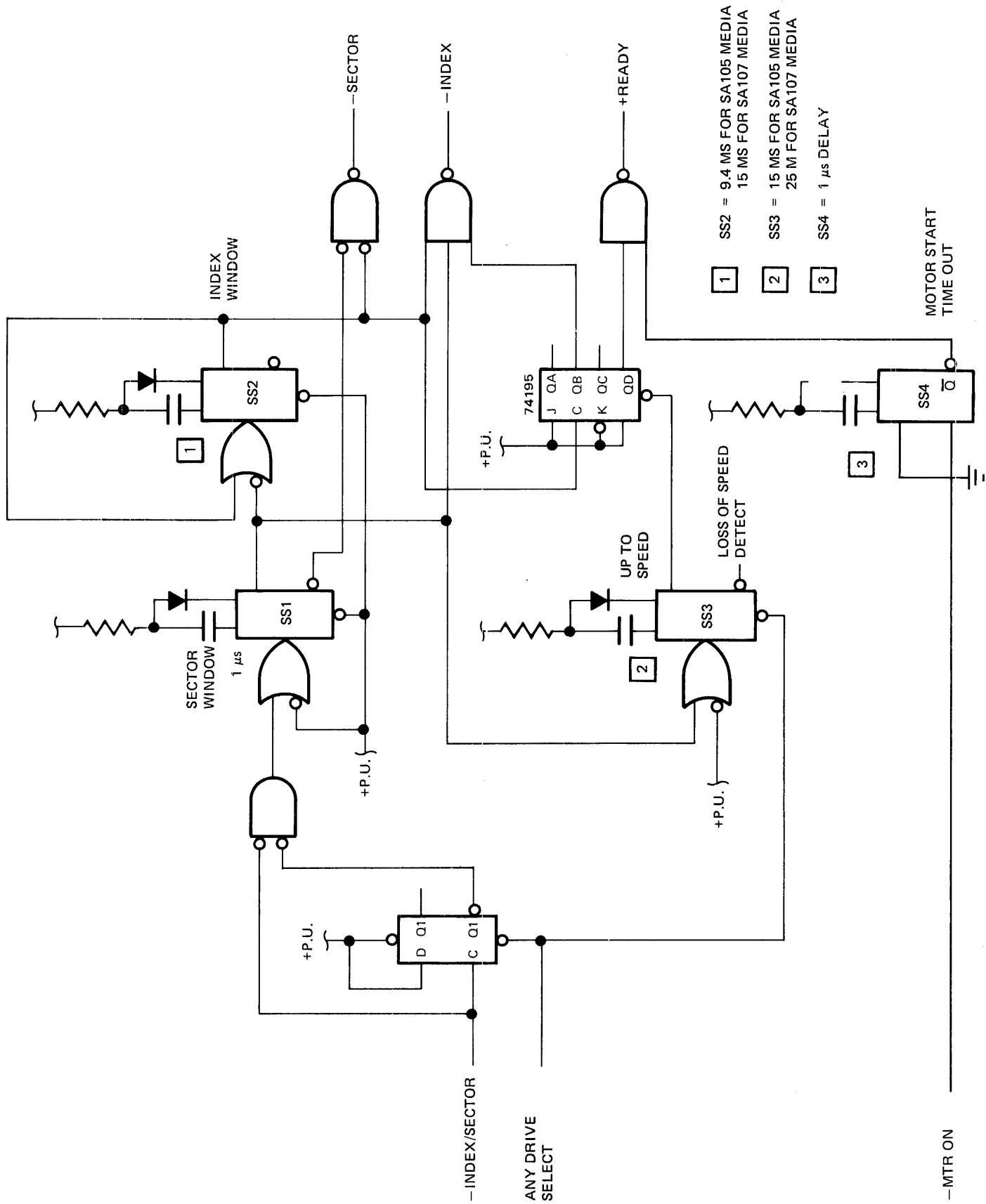
FIGURE 33. CRC GENERATION
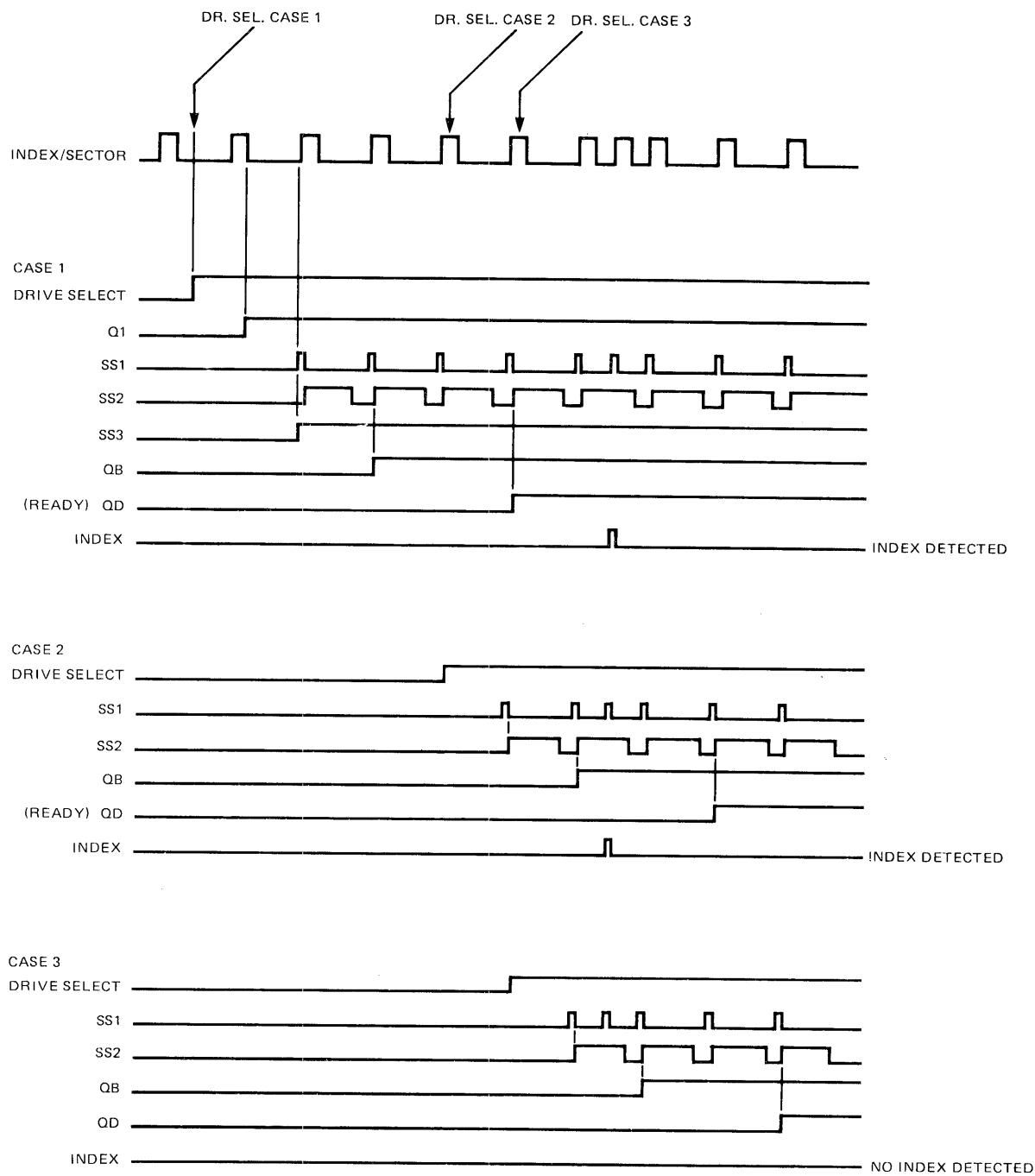
FIGURE 34. INDEX/SECTOR SEPARATOR AND READY CIRCUIT
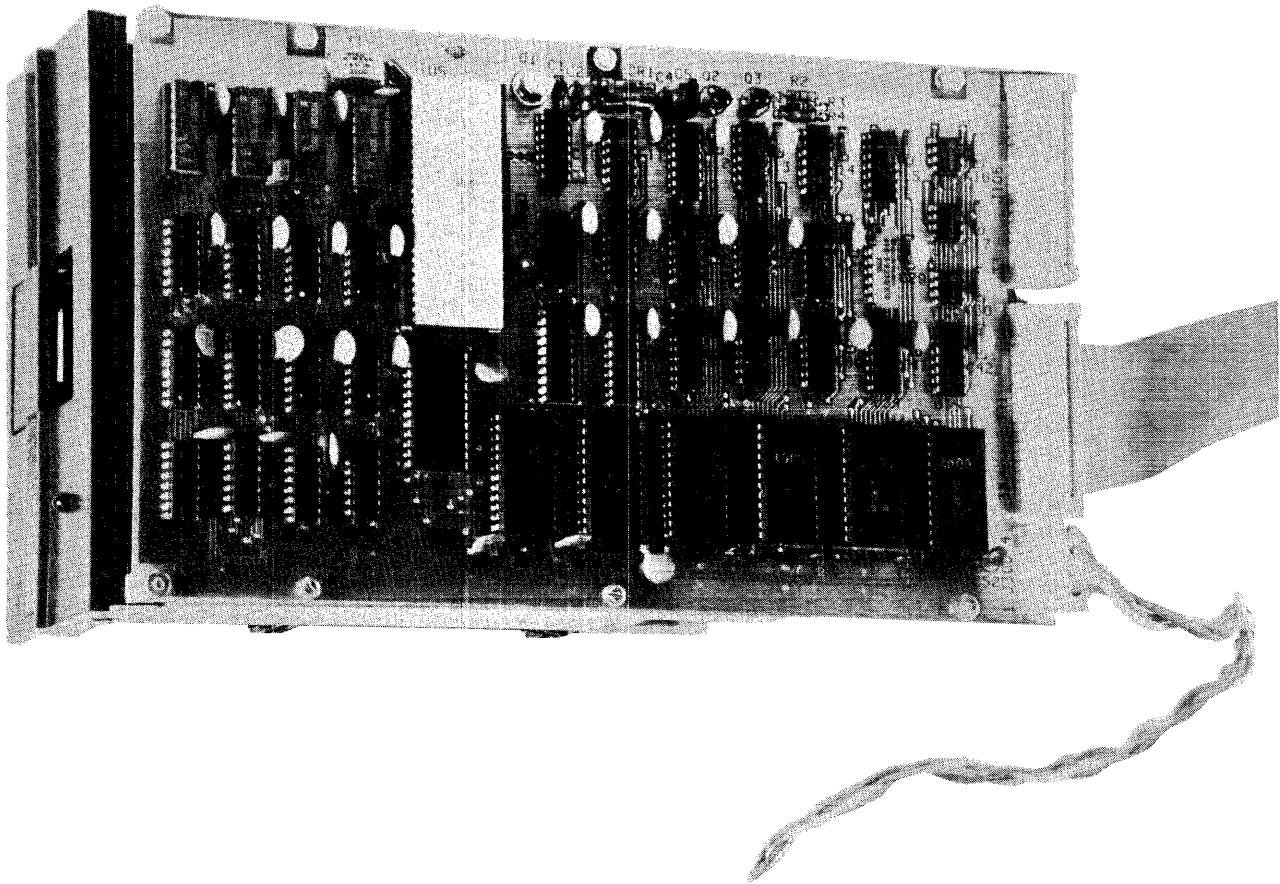
36

FIGURE 35. INDEX/SECTOR TIMING

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FIGURE 36. SA400 WITH SA4400 CONTROLER

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9.0 OPERATION PROCEDURES

The SA400 was designed for ease of operator use to facilitate a wide range of operator orientated applications. The following section is a guide for the handling procedures on the minidiskette and minifloppy drive.

9.1 Minidiskette Loading

Figure 37 shows the proper method of loading a minidiskette in the SA400. To load the diskette, open the door on the front panel, insert the diskette with label towards the door handle and close handle. A mechanical interlock prevents door closure without proper media insertion, thus eliminating media damage.
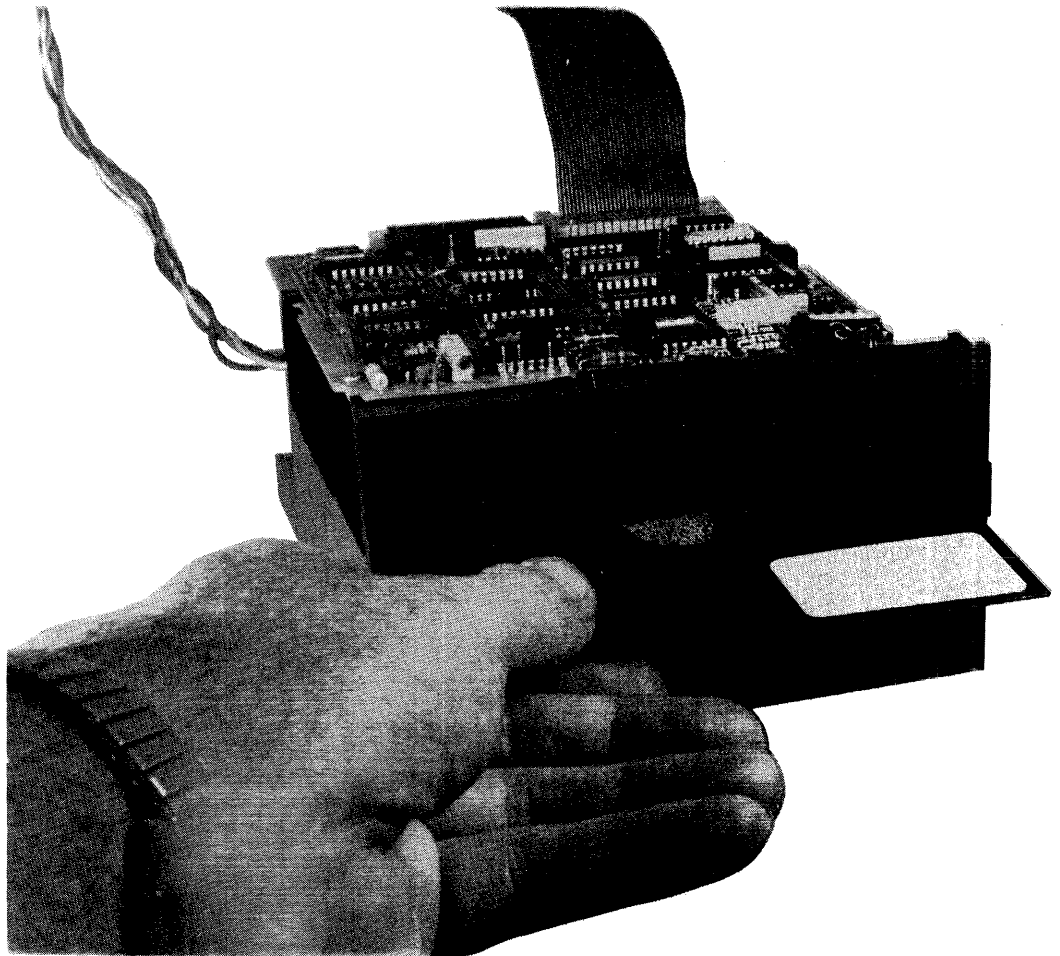

FIGURE 37. LOADING SA400

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9.2 Minidiskette Handling

To protect the diskette, the same care and handling procedures specified for computer magnetic tape apply. These precautionary procedures are as follows:

1. Return the diskette to its storage envelope whenever it is removed from file.

2. Keep cartridges away from magnetic fields and from ferromagnetic materials which might become magnetized. Strong magnetic fields can distort recorded data on the disk.

3. Replace storage envelopes when they become worn, cracked or distorted. Envelopes are designed to protect the disk.

4. Do not write on the plastic jacket with a lead pencil or ball-point pen. Use a felt tip pen.

5. Heat and contamination from a carelessly dropped ash can damage the disk.

6. Do not expose diskette to heat or sunlight.

7. Do not touch or attempt to clean the disk surface. Abrasions may cause loss of stored data.

9.3 Write Protect Feature

The SA104/105 minidiskettes have the capability of being write protected. A write protect notch is located on the diskette jacket. When the notch is open writing is allowed. When the notch is covered with a tab, writing is inhibited and the interface signal will be activated. Figure 37 illustrates the SA104/105 minidiskette write protected and unprotected.
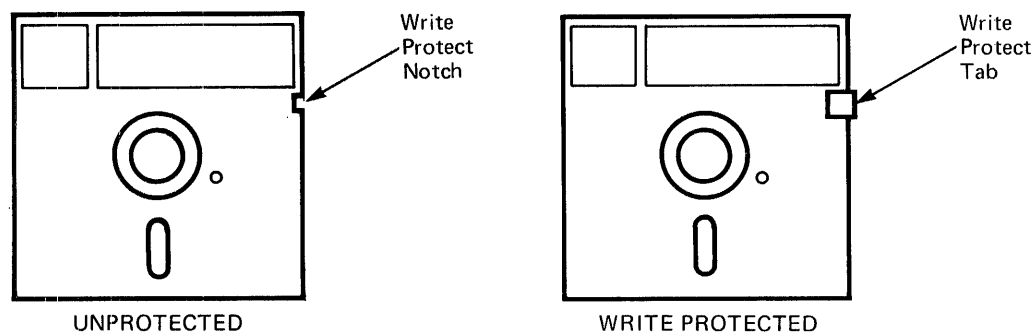
UNPROTECTED

Write Protect Notch

WRITE PROTECTED

Write Protect Tab

FIGURE 37. SA104/105 WRITE PROTECT

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